3er FORO INTERNACIONAL DE TV DIGITAL DE LA HABANA

DIGITAL SYSTEM DESIGN FOR A DTMB MODULATOR

Author:
Eng. Reinier Díaz Hernández
reinier@lacetel.cu

LACETEL: Technological transference process

LACETEL's previous works on DTMB assimilation and reproduction

- *BSc Thesis: Design of Scrambler, channel coding, mapping and interleaving for DTMB modulator. 2011.*
- *MSc Thesis: Design and implementation of 3780 points Fast Fourier Transform for DTMB standard. 2012.*
- *BSc Thesis: Design and Implementation of IP modules for a DTMB modulator. 2014.*
- *IBERCHIP XXI WORKSHOP: Reference model for a DTMB Modulator. 2015*


Modelo de referencia de un modulador de la norma DTMB de Televisión Digital

Reinier Díaz Hernández
LACETEL, Instituto de Investigación y Desarrollo de Telecomunicaciones
La Habana, Cuba
reinier@lacetel.cu

Ernesto Fontes Pupo
LACETEL, Instituto de Investigación y Desarrollo de Telecomunicaciones
La Habana, Cuba
fonts@lacetel.cu

Problematic Situation

- *There are available previous HW designs developed in LACETEL that implements different blocks of a DTMB modulator. They were made independently and don't have a system design approach. Because of that its interfaces are not compatibles to each other, making difficult its integration as a system.*
- *There is a verified functional reference model of a DTMB compliant modulator oriented to software simulation of the system but not directly applicable to a HW implementation.*
- *So, it is needed a system design for Hardware implementation of a DTMB modulator that allows to utilize previous experiences and integrate previous designs in a modular approach.*

Objectives

- *To select a digital system design approach that facilitates to reutilize previous designed blocks and integrates them as independent units with standardized interfaces.*
- *To design a hardware system that implements a modulator according to DTMB standard.*
- *To validate the created design by simulation and by Hardware-Software co-simulation.*

Different DSP systems design approach

- *Fully synchronous custom design*
  - *Highly optimized final implementation*
  - *Complex design process since each modulation mode should be independently designed and synchronized.*
  - *Centralized timing and control, makes difficult to modify internal blocks (optimization or new working modes due to Standard evolution)*

Different DSP systems design approach

- *Modular design with FIFO interfaces*
  - *Simplest design process, each block independently designed and easy to synchronize with the system*
  - *High consumption of memory resources*
  - *Distributed timing and control through each block, facilitates to modify block's internal design (optimization or new working modes due to Standard evolution)*

Different DSP systems design approach

- *Modular design with self-timing handshaking protocols and interfaces*
  - *Relative simple system design process. Each block is responsible to synchronize with the system. Results on one design that dynamically accommodates different data rates in response to changing operation modes.*
  - *Distributed timing and control through each block, facilitates to modify block's internal design (optimization or new working modes due to Standard evolution)*
  - *Additional resource consumption for handshaking circuits.*

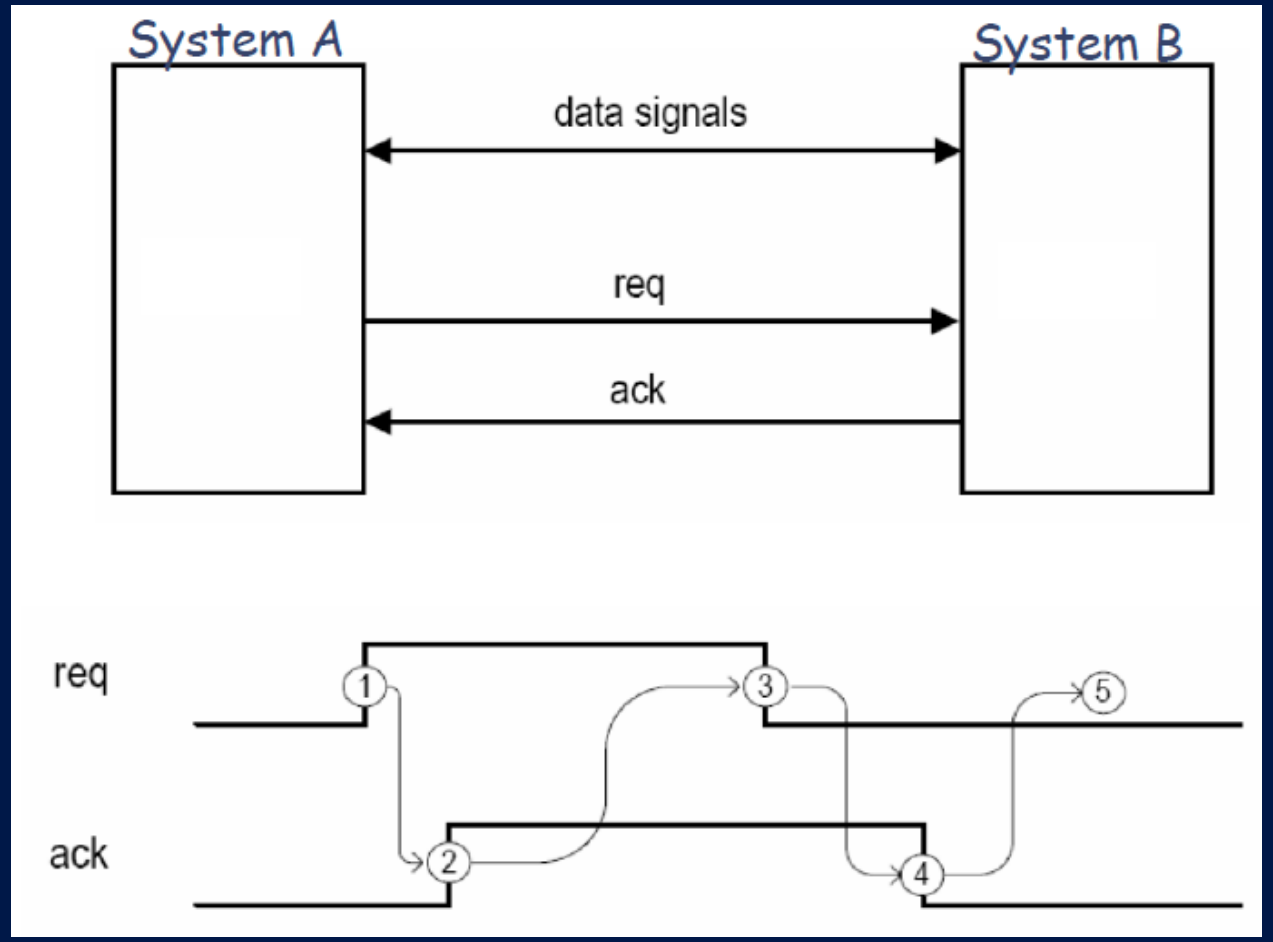
Selected design approach

- *External FIFO interfaces to isolate internal implementation and timing from external inputs/outputs of the FPGA.*
- *Internal implementation based upon Modular design with self-timing handshaking protocols and interfaces*
- *Incremental design process (in each stage of design a new block is added, all with common interfaces).*

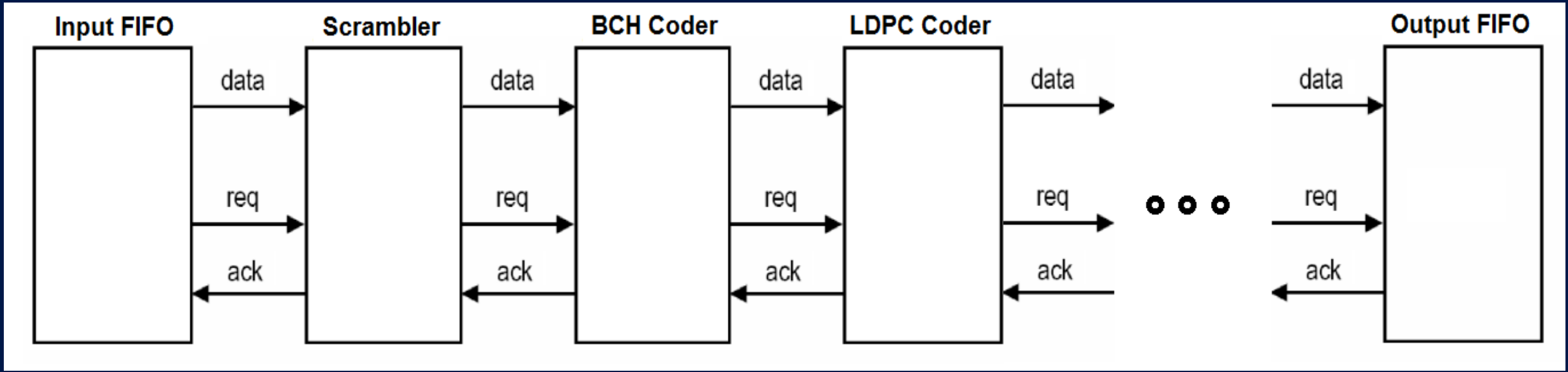
Four Phases Synchronization protocol

1. *Tx activates the request.*
2. *Rx activates the acknowledge of the request*
3. *Tx de-activates the request*
4. *Rx deactivates the acknowledge*

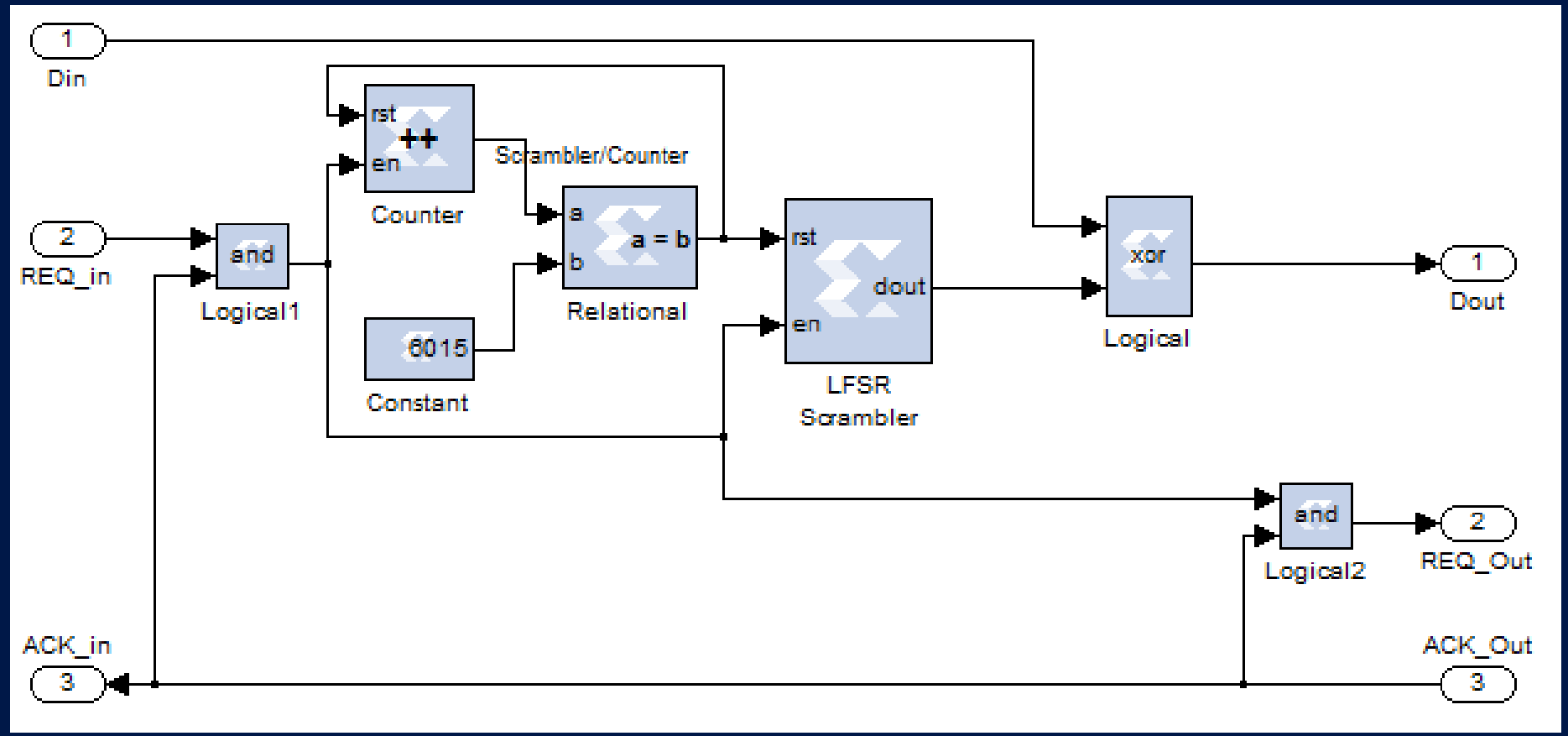
➢ *Tx can start a new request*



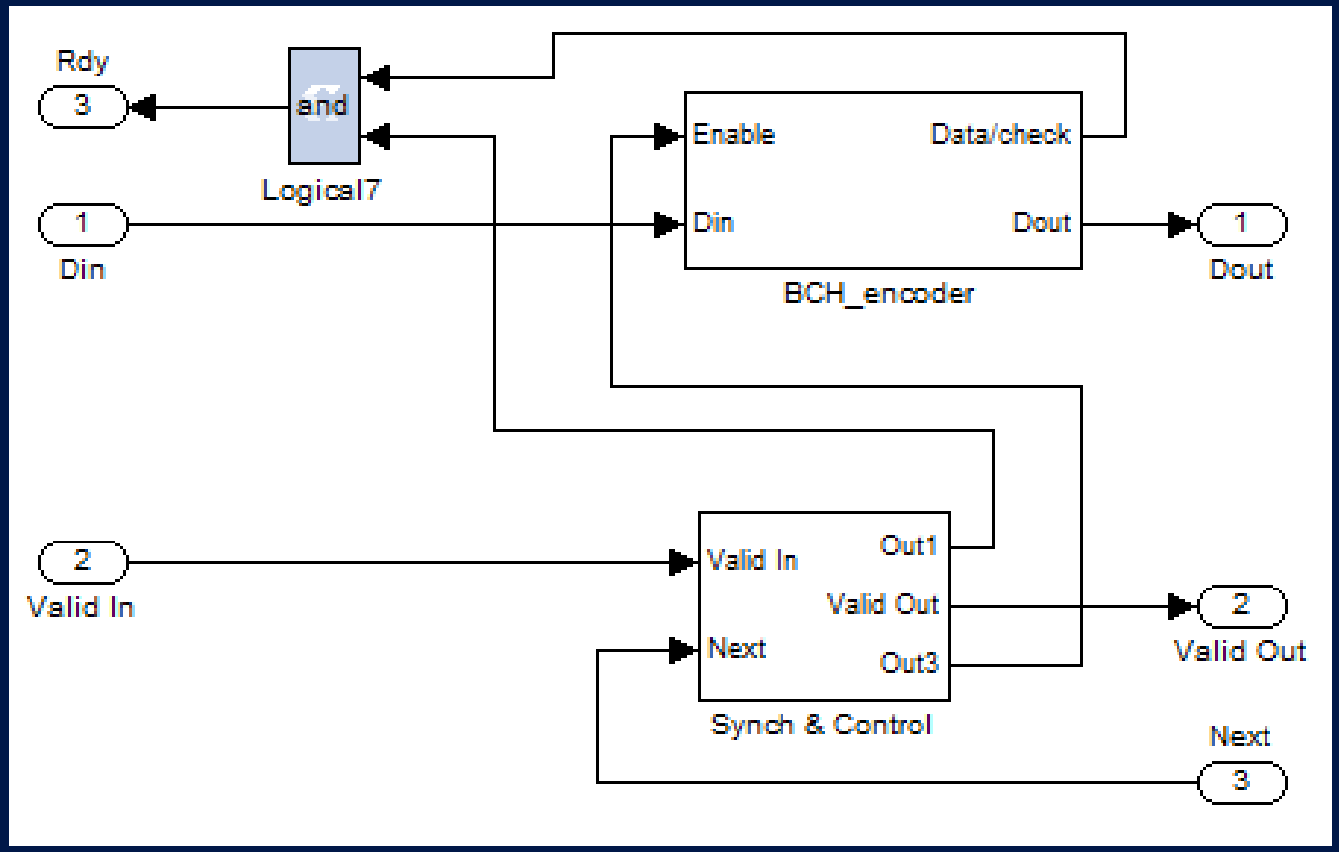
Implemented Design



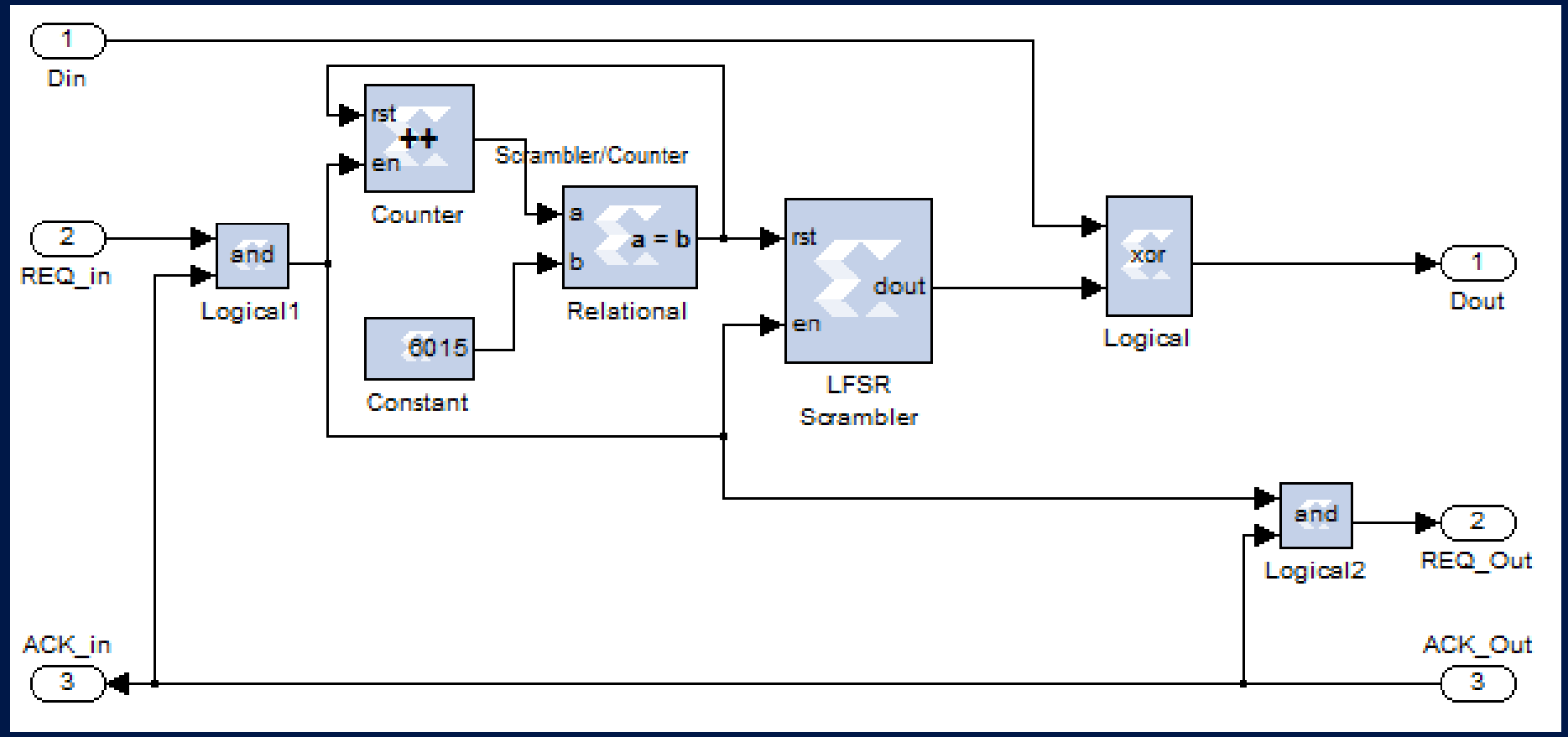
Scrambler internal structure



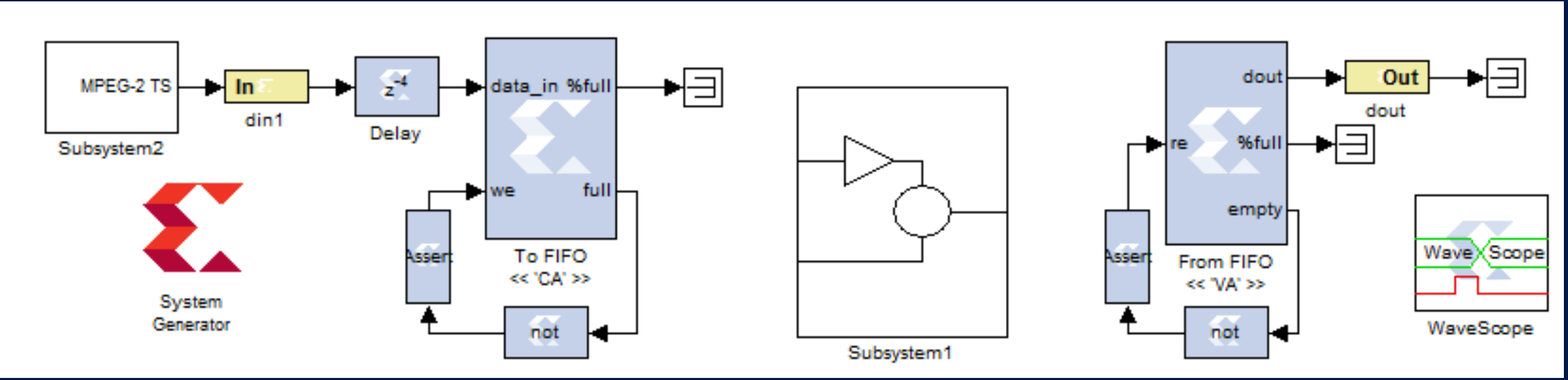
BCH Coder internal structure



LDPC internal structure



Simulation Testbench



Conclusions

- *The present work describes a System Design for a DTMB modulator.*
- *The design was validated by simulation and HW-cosimulation.*
- *The Simulink environment with Xilinx System Generator tools used for this design facilitates the design process as well as the validation stage*

DIGITAL TELEVISION LABORATORY

www.lacetel.cu