RESEARCH & DEVELOPMENT TELECOMMUNICATION'S INSTITUTE

Optimization proposal for an FPGA-based H.264/AVC decoder model

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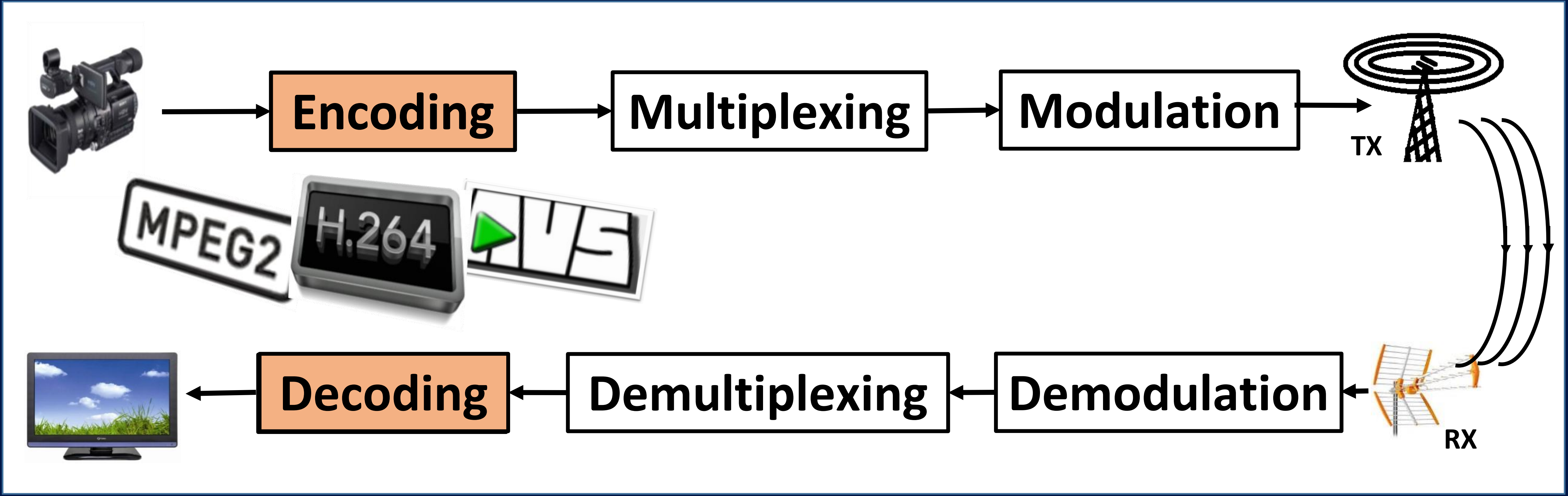
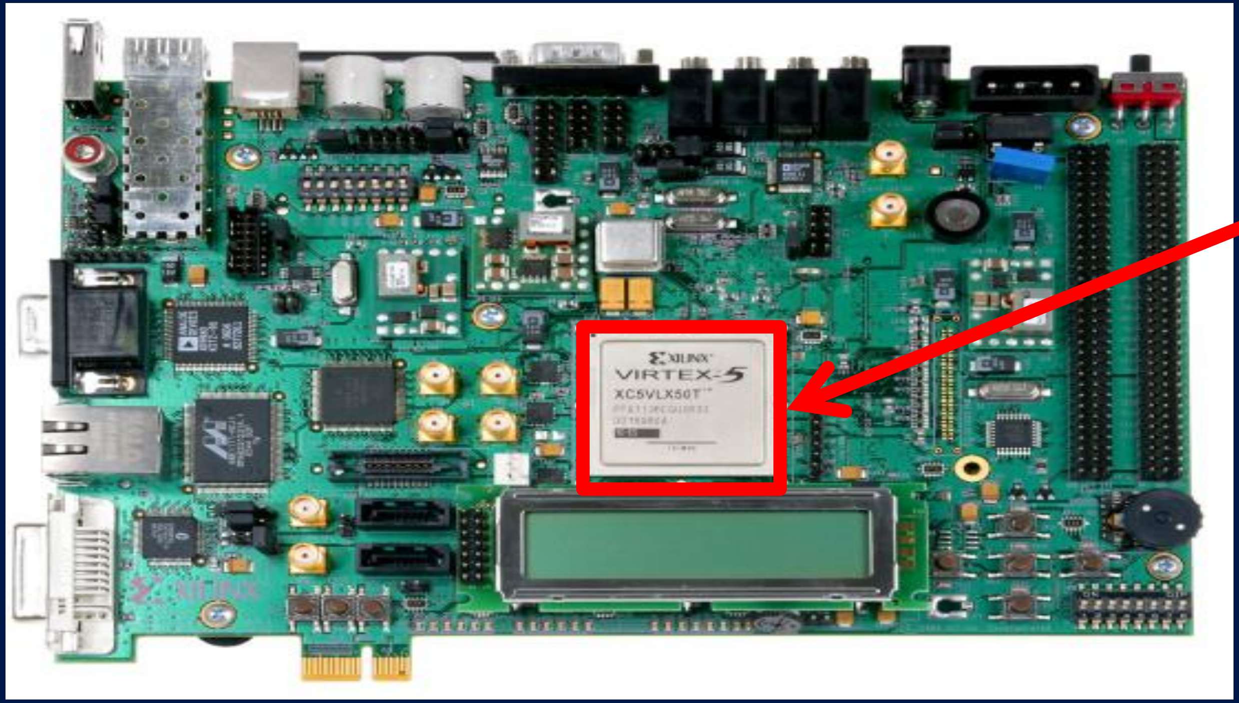
Introduction (1/3)

Digital Terrestrial Television System



Introduction (2/3)

FPGA software/hardware co-design for the H.264/AVC decoder implemented in ***LACETEL***



Xilinx ML507 evaluation board

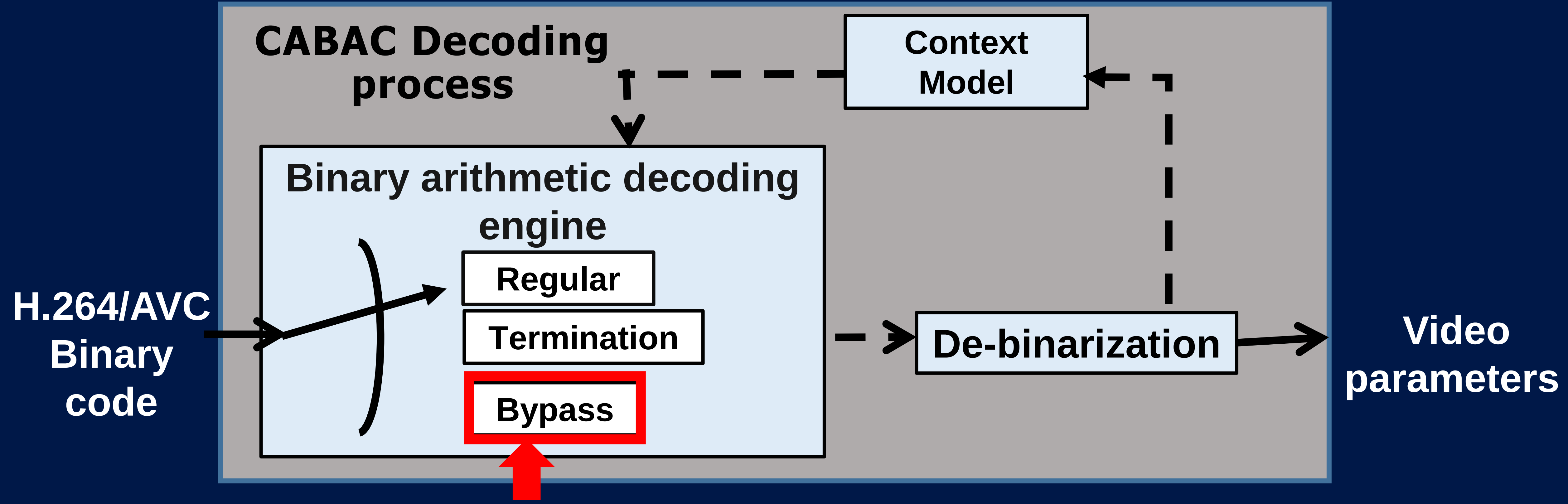
Embedded system on a Xilinx Virtex 5 FPGA.

The H.264/AVC decoder software is run on the PowerPC processor

The communication between the PowerPC processor and the hardware is done over PLB bus.

Introduction (3/3)

Bypass decoding



Bypass Decoding IP module implemented in VHDL, in 2014

Problematic Situation

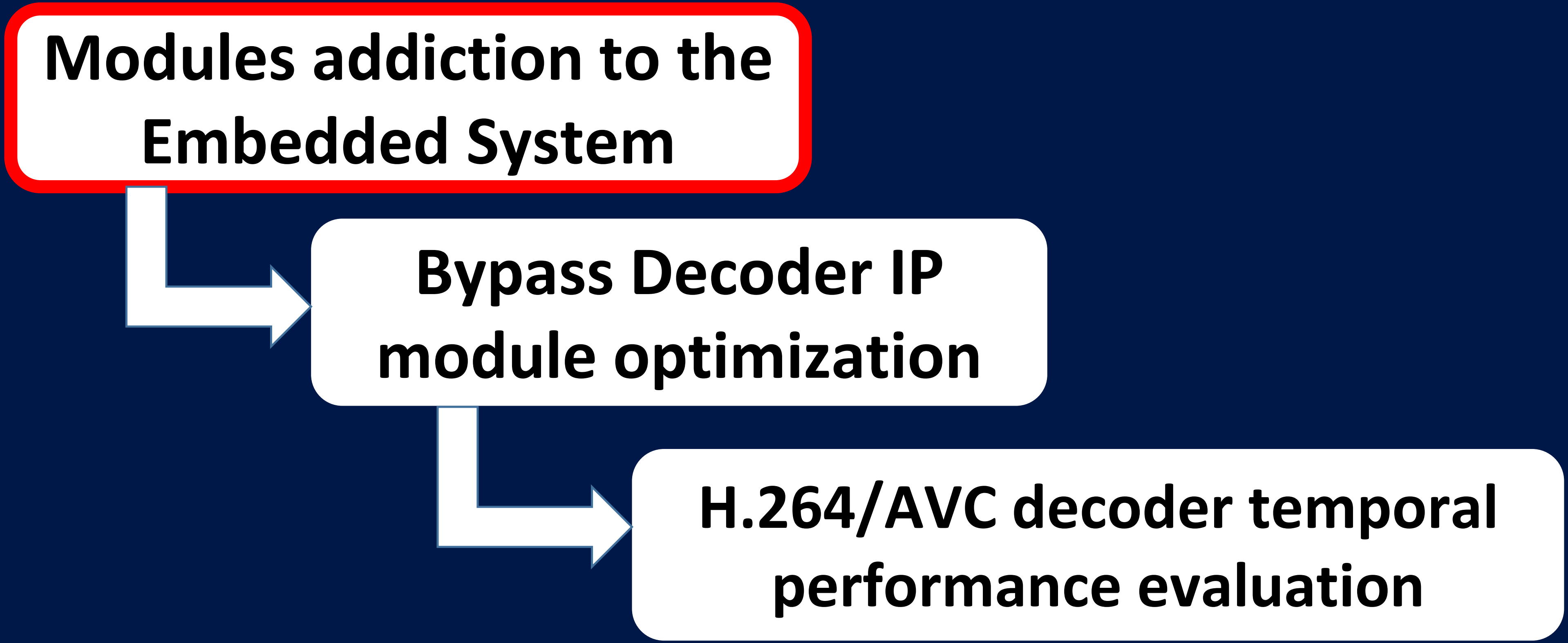
The FPGA-based H.264/AVC decoder implemented in ***LACETEL:***

- does not meet time requirements to become a practical final solution.
- does not have complementary tools to identify and experiment with blocks that are critical in terms of speed.

Main Goal

Insert the Bypass Arithmetic Decoding IP module of CABAC in the H.264/AVC decoder model, and necessary timing tools to evaluate the system behavior.

Design flow

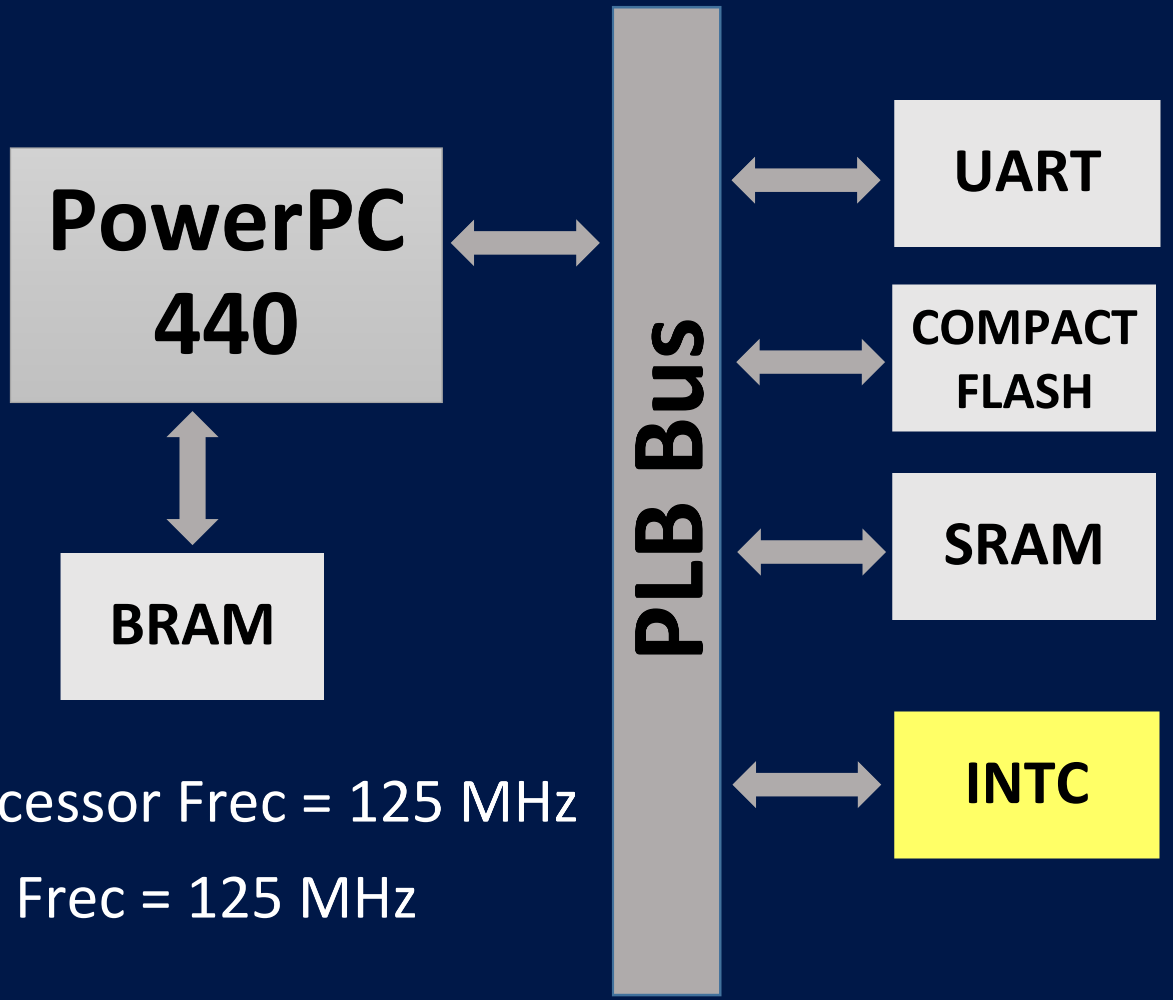


Modules addiction to the Embedded System

Bypass Decoder IP module optimization

H.264/AVC decoder temporal performance evaluation

modules addiction to the embedded system (1/3)



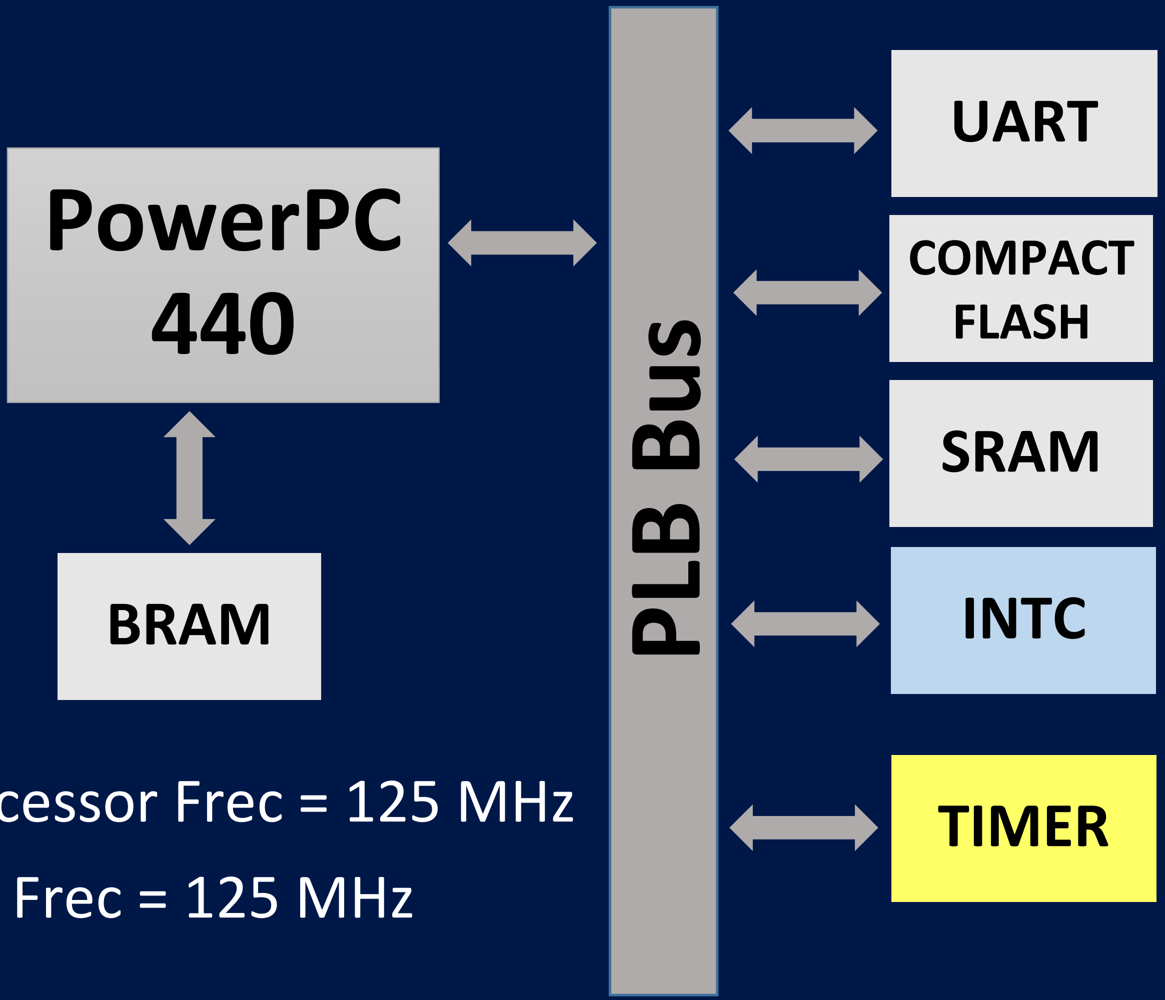
Processor Frec = 125 MHz

Bus Frec = 125 MHz

Interrupt Controller

- Connected as a 32 bits slave of Bus PLB.
- Two interrupt inputs used.
- Single interrupt output.
- Priority between interrupt requests determined.
- Each input configured for rising edge sensitivity.

modules addiction to the embedded system (2/3)



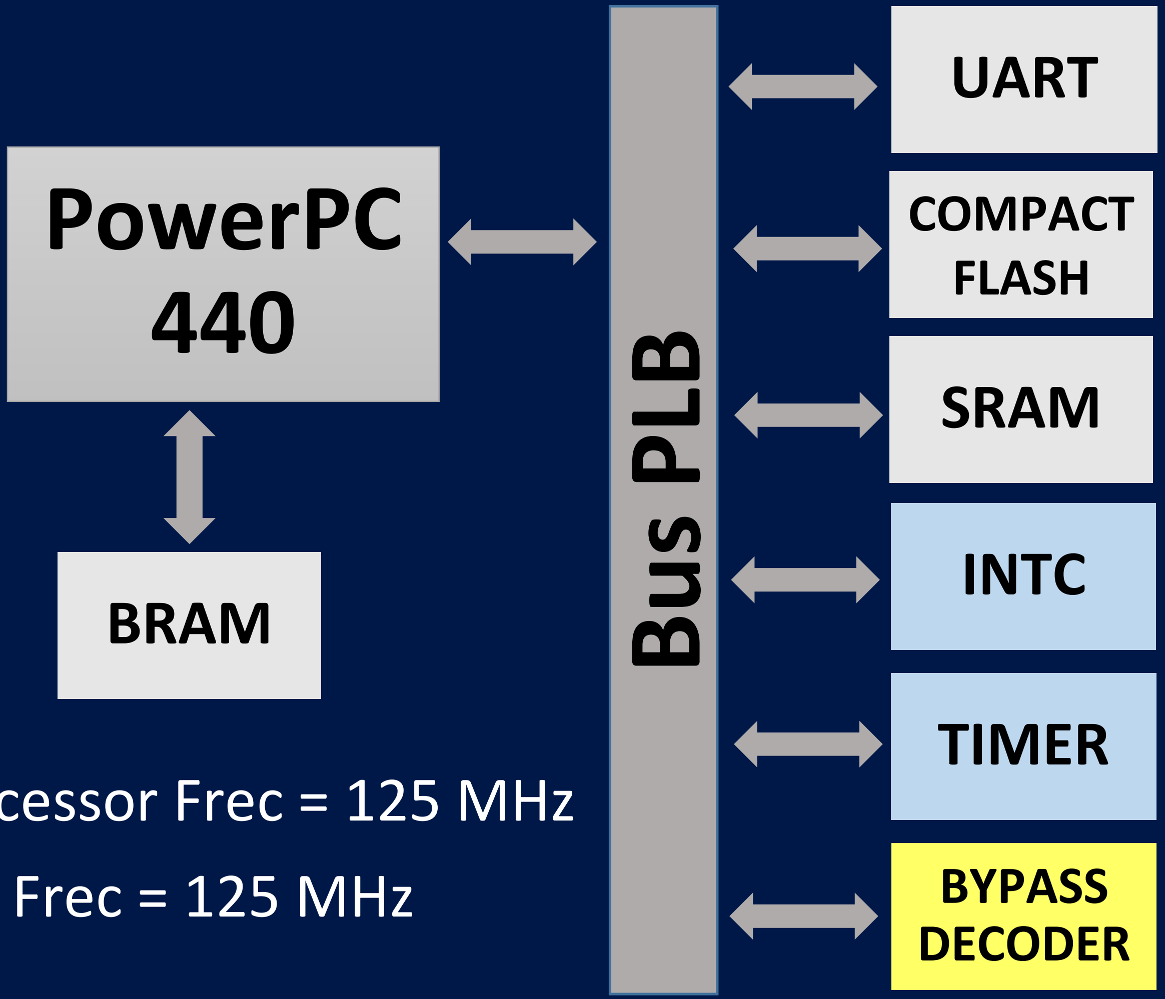
Processor Frec = 125 MHz

Bus Frec = 125 MHz

Timer/Counter

- Connected as a 32 bits slave of Bus PLB.
- Configured in Generation Mode.
- Interrupt output signal to the interrupt controller.

modules addiction to the embedded system (3/3)



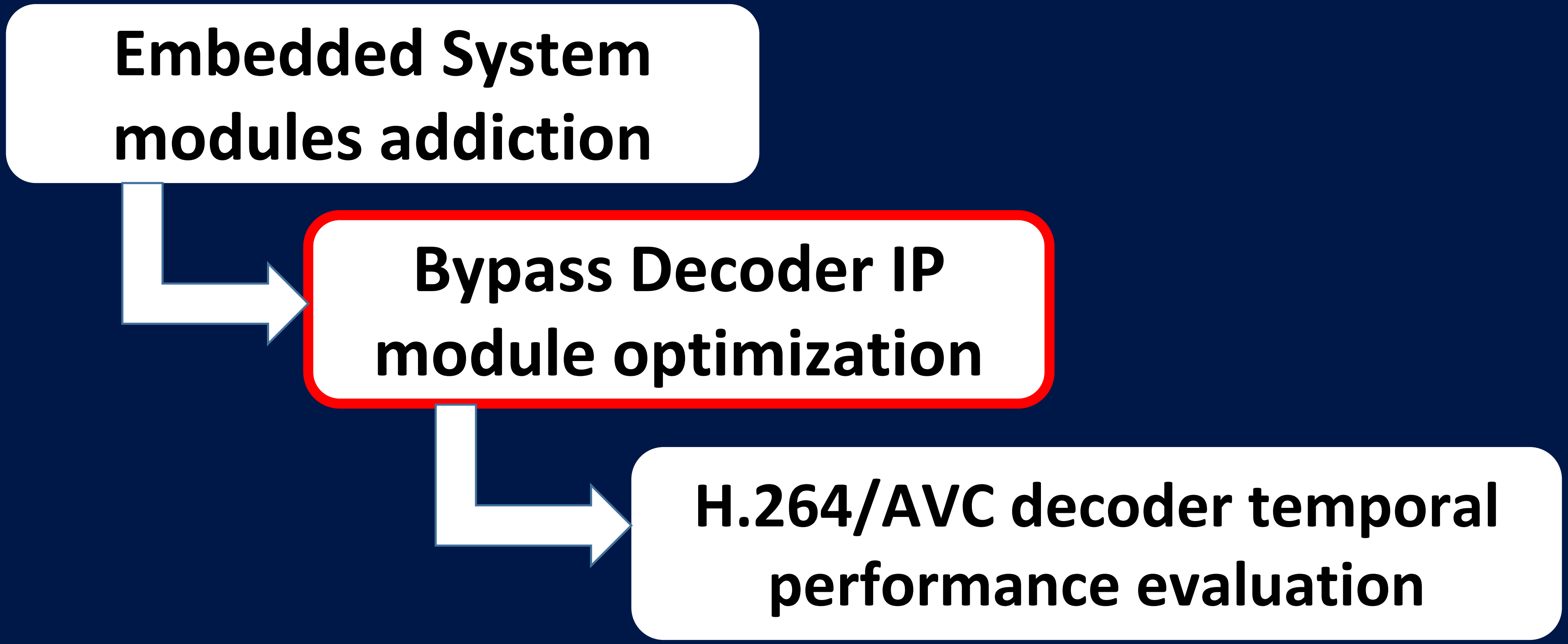
Processor Frec = 125 MHz

Bus Frec = 125 MHz

Bypass Decoder IP module

Hardware module in charge of doing bypass decoding of CABAC.

Design flow



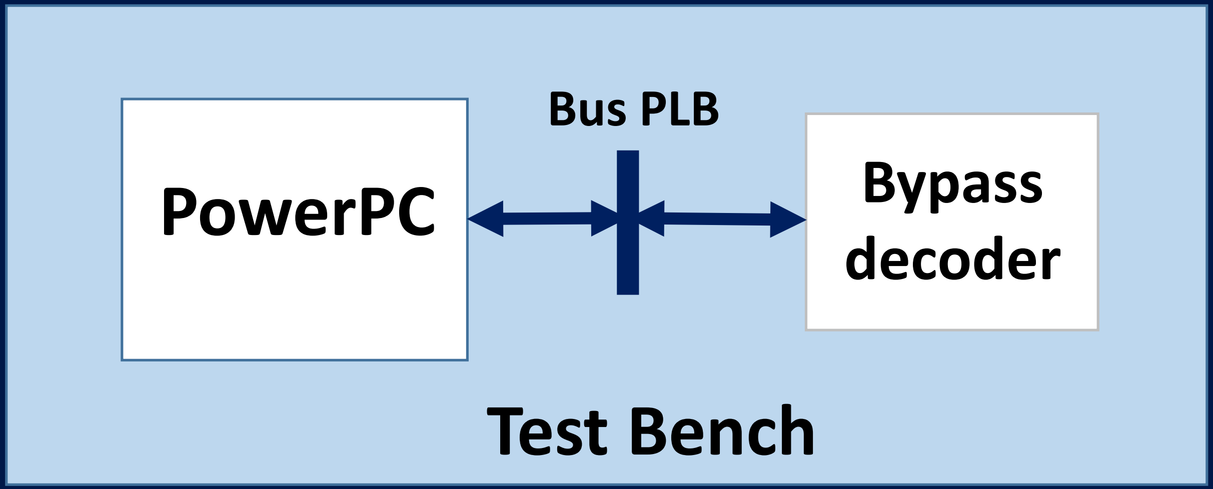
Embedded System modules addiction

Bypass Decoder IP module optimization

H.264/AVC decoder temporal performance evaluation

Decoder Bypass IP module previous implementation

- Implemented in a test system with the PowerPC processor and the PLB Bus.
- The processor polls the module's outputs to know when the values are ready.



Bypass Decoder IP module optimization (1/3)

Decoder Bypass IP module previous implementation:

- Twelve software registers
- Single intern signal in each register

Decoder Bypass IP module optimized:

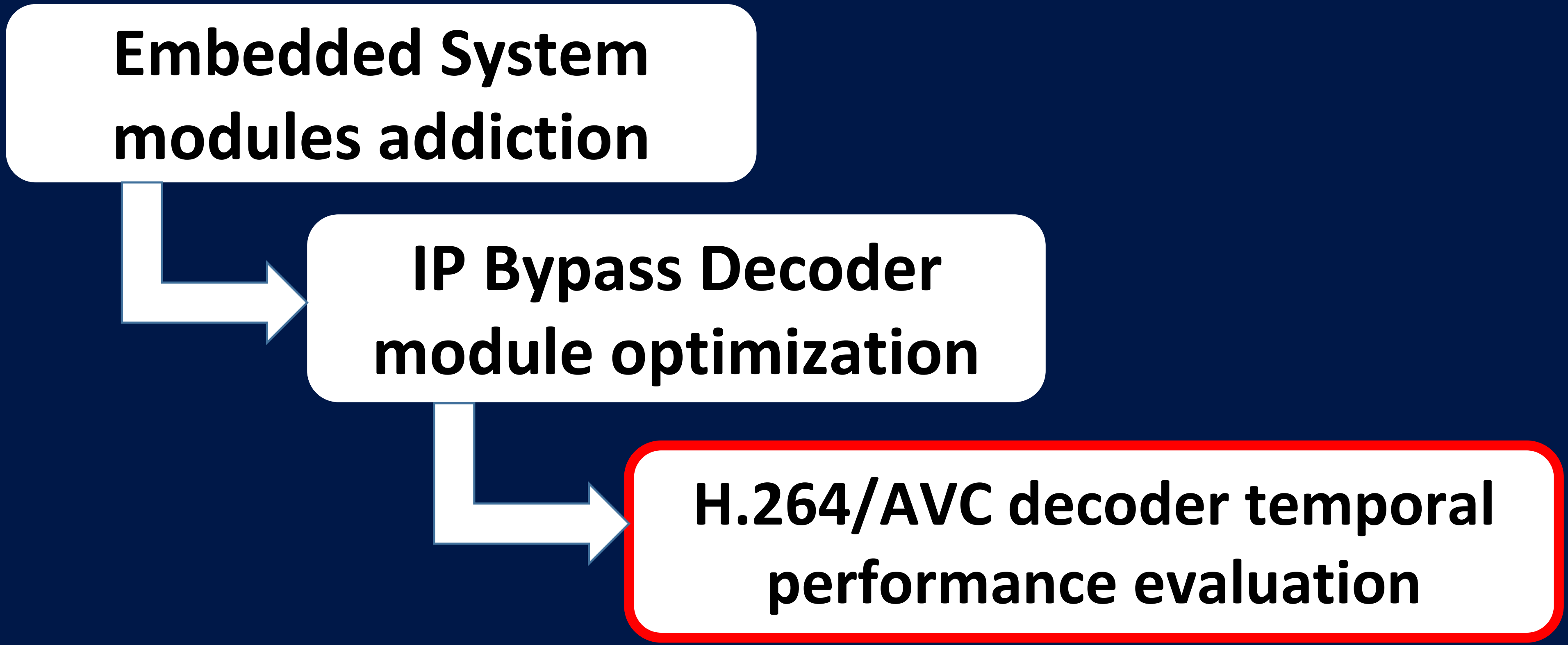
- Six software registers.
- Many intern signals in each register.
- Memory consumption reduced.

Bypass Decoder IP module optimization (3/3)

Bypass Decoder IP module processing time 9,6 ns	<	PLB single data beat read time 32 ns

It is possible just to read and write the data from processor to the Bypass IP module without using any method like the poll or the interruption.

Design flow



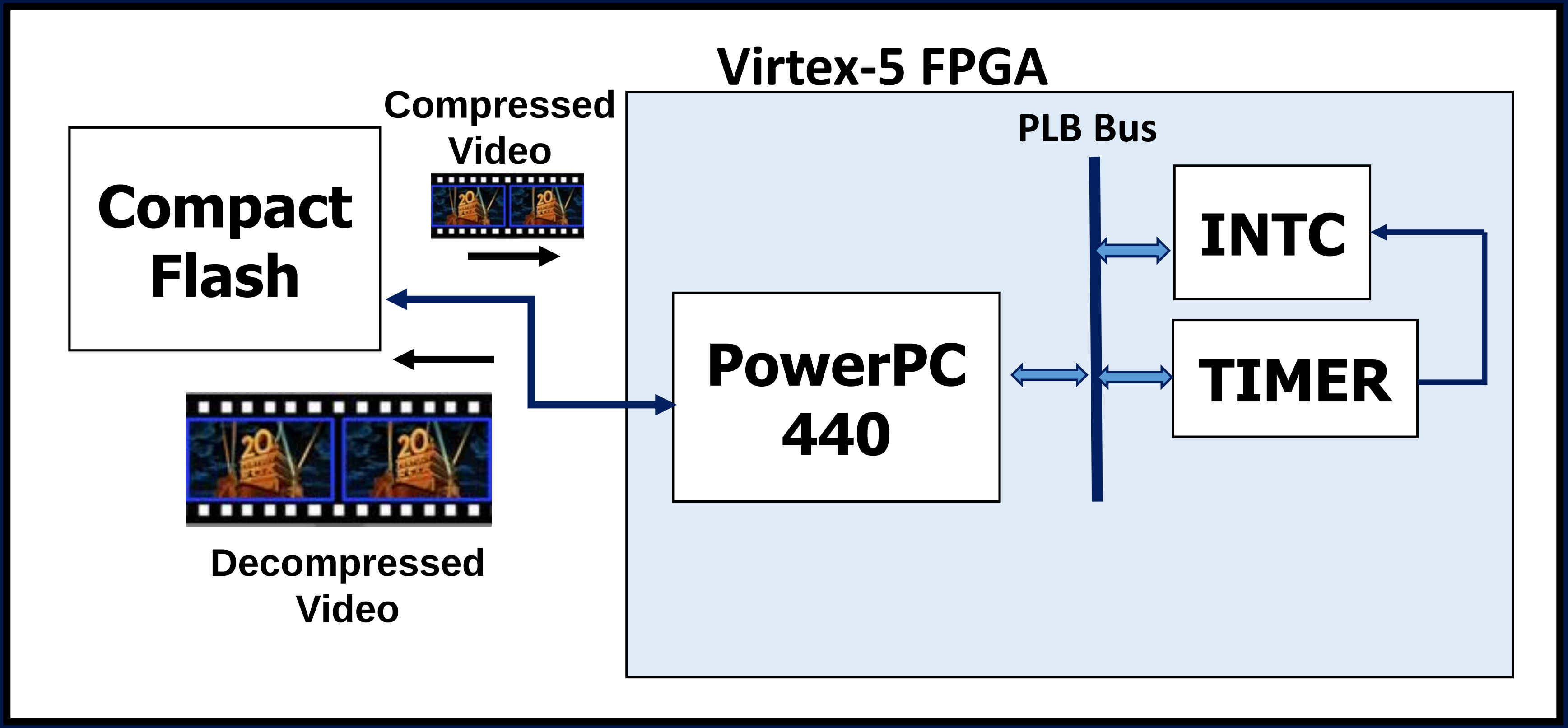
Embedded System modules addiction

IP Bypass Decoder module optimization

H.264/AVC decoder temporal performance evaluation

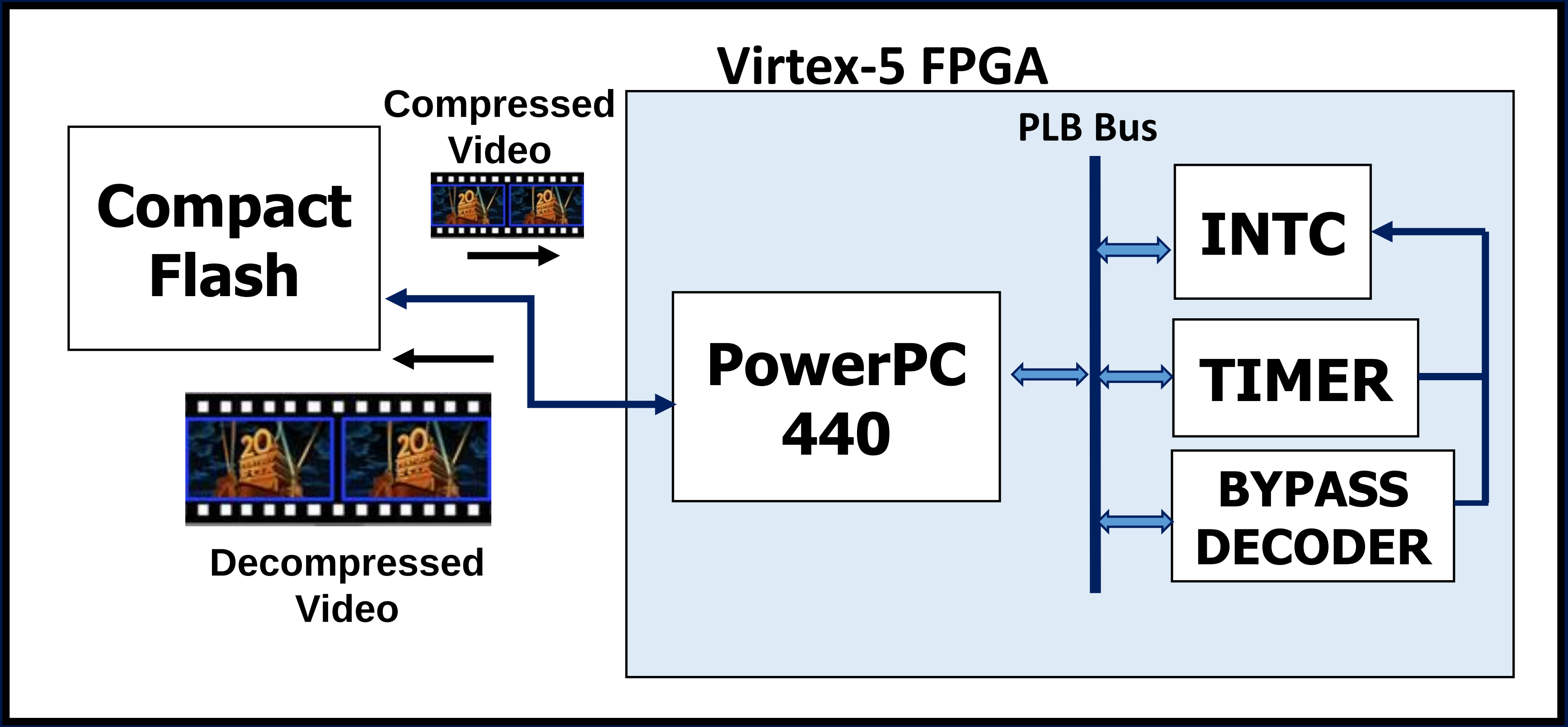
H.264/AVC Decoder temporal performance evaluation (1/3)

Experiment 1: Software H.264/AVC Decoding Timing (previous work in *LACETEL*)



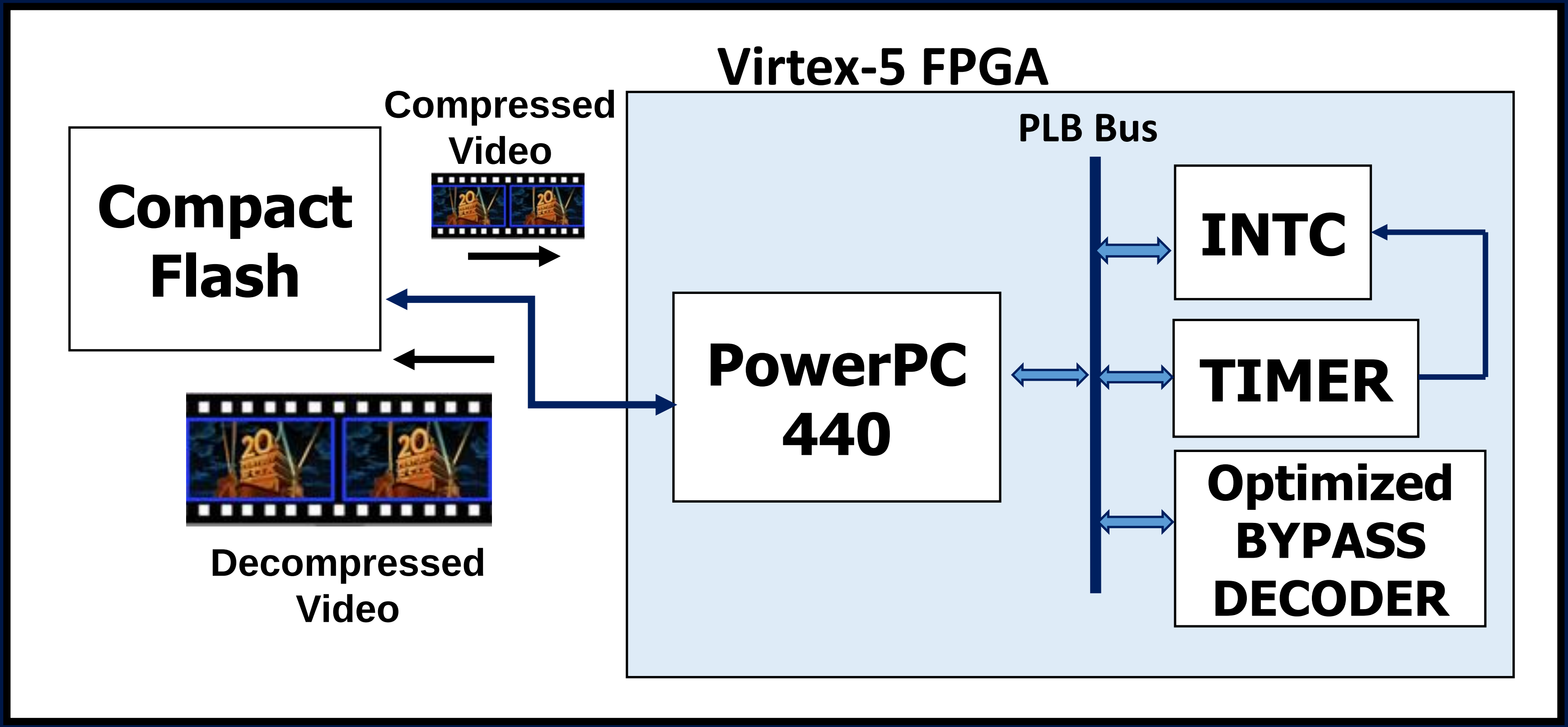
H.264/AVC Decoder temporal performance evaluation (2/3)

Experiment 2: Software/Hardware H.264/AVC Decoding Timing (with Bypass Decoder IP module on)



H.264/AVC Decoder temporal performance evaluation (3/3)

Experiment 3: Software/Hardware H.264/AVC Decoding Timing (with optimized Bypass Decoder IP module on)



H.264/AVC Decoder temporal performance evaluation (3/3)

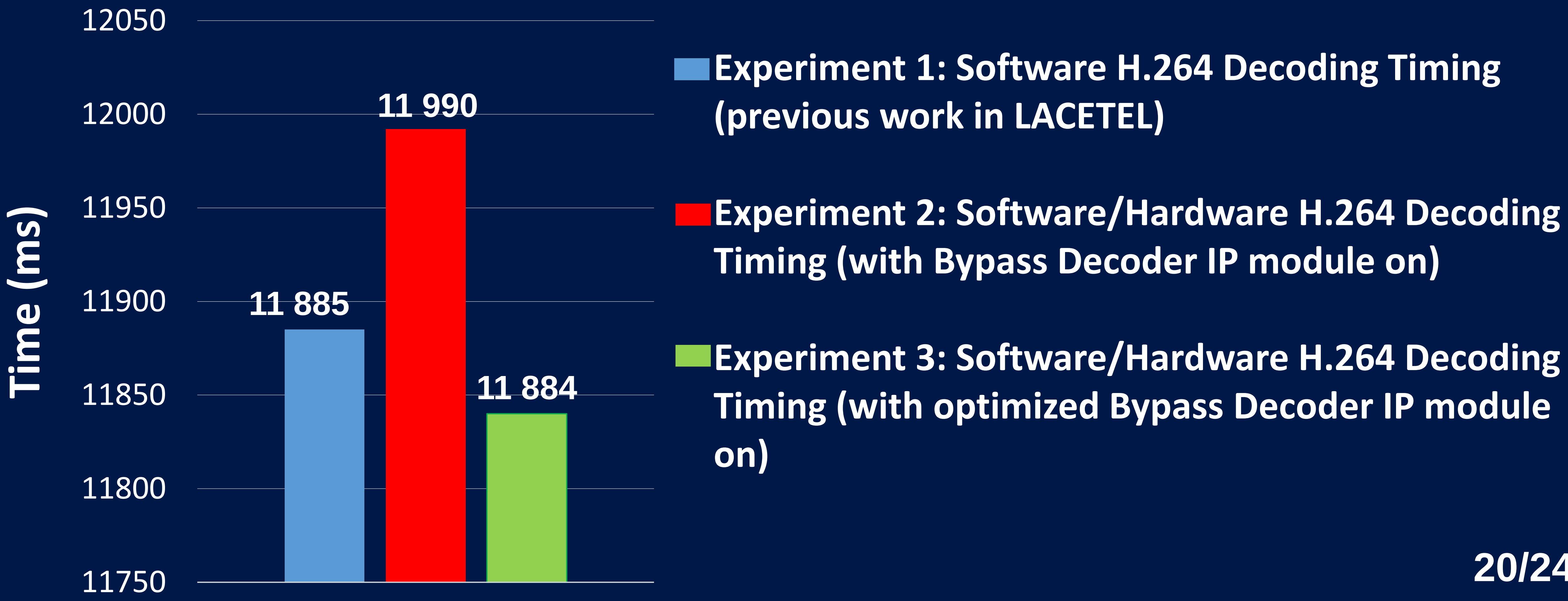
Xilinx Software Development Kit

H.264/AVC Video	Resolution	Frames	Profile
Video_1	176 x 144	3	Main
Video_2	352 x 240	8	High
Video_3	176 x 144	10	High 4:2:0

$$Time = \frac{gotten\_value+max\ \_cont*tmr\_overflow}{bus\_frec}$$

Analysis of experiments results

Results for Video_2



🟦 Experiment 1: Software H.264 Decoding Timing (previous work in LACETEL)

🟥 Experiment 2: Software/Hardware H.264 Decoding Timing (with Bypass Decoder IP module on)

🟩 Experiment 3: Software/Hardware H.264 Decoding Timing (with optimized Bypass Decoder IP module on)

Conclusions (1/2)

- The Interrupt controller and the Timer/Counter were added to the embedded system in which the H.264/AVC model is implemented.
- The Bypass Decoder IP module was optimized and fitted into the H.264/AVC decoder system.
- The H.264/AVC Decoder temporal performance was evaluated for different designs and the results showed that the optimization of Bypass Decoder IP module made possible to reduce decoding delay.

Conclusions (2/2)

- A methodology of IP modules insertion into the H.264/AVC decoder in an embedded system was build.
- The H.264/AVC decoder showed is a platform capable of supporting next implementations such as the insertion of IP modules following the way showed in this work.

Next work

- Introduce some IP modules into the H.264/AVC decoder system that allow to visualize the decoded frames through interfaces such as VGA or DVI.
- Time the delay produced by the rest of the elements in the H.264/AVC Decoder System to find which of them need to be optimized.

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