5th Digital Television Forum

Hardware Implementation of Min-Sum Algorithm for LDPC Decoding

Eng. Osmay Yaunner Núñez
MSc. Reinier Díaz Hernández
Eng. Ernesto Fontes Pupo

November, 2017
Introduction
Introduction

- DTMB TVD Transmission-Reception simulation model implemented in MATLAB, developed by LACETEL.
- Allows characterization and analysis of DTMB standard performance.
- LDPC decoding was identified as critical processing stage.
Purpose

- To reduce LDPC decoding simulation time on the DTMB model developed in MATLAB.
Simplified DTMB Model BD

Binary Generator → BCH Encoder → Codificador LDPC → Symbol Mapping → OFDM Tx

BER calculation → BCH Decoder → Hardware LDPC Decoder → Symbol Demapping → OFDM Rx

BER calculation → BCH Decoder → Hardware LDPC Decoder

AWGN
Goals

First stage
- To design the block diagram of the LDPC decoder.
- To implement an LDPC hardware decoder using VHDL.

Second stage
- To insert the LDPC hardware decoder on an FPGA.
- To integrate the hardware design with the DTMB simulation model using hardware co-simulation.
- To perform time measurements.
Basic Digital Communication System

(Shannon, 1948)
LDPC Codes

- Near Shannon Limit Error-Correcting codes.
- Linear block codes.
- First introduced in 1962.
- “Retomados” in the 90’s
- Applications: DTV, WiFi, Satellite Communications, Ethernet, etc.
LDPC Decoding (1/2)

- Iterative Process that involves the calculation of probabilistic information on each iteration.

- There are different algorithms depending on the type of operation that it is performed.

- LLR: Probability Estimation
  - sign: indicates whether the decoded bit is a 1 or a 0.
  - magnitude: indicates the reliability of the estimation.
It is described graphically as two node sets that perform computations in parallel, then communicate with each other over pre-defined connections.
Hardware Resources

- Desktop PC
- ML507 Evaluation Board
  - XC5VFX70T FPGA
  - 9 Mb SRAM
  - 2 x 32Mb Flash PROM
- Memory Requirement:
  - LLR: 64 kb
  - Parity Check Matrix: 40 kb
LDPC Decoder General Structure

- Memoria
- Cálculo Síndrome
- Estimación código
- Chequeo Síndrome
- Control Iteraciones

Diagrama de flujo:
- LLR entrada
- Matriz Chequeo
- Temp Bits
- Temp
- Iteraciones
- Stop
- Iter_new
- Bits dec final
- Iteraciones final
- Memoria
- LLR iteraciones
- Enable_iteraciones
- Procesam. Nodo de Variable
- Procesam. Nodo de Chequeo
- Enable_iteraciones
- LLR entrada
- LLR iteraciones
- Enable_iteraciones
Validation

- Functional Verification
- Post-synthesis Verification (functional and temporary)
- Post-Place and Route Verification
Current Work

- Architecture selection for check and variable node processing blocks.
- Hardware implementation of matrix-vector multiplication (syndrome computation block)
Typical Hardware Architectures

- **Totally Parallel (TP):** All variable nodes, check nodes and its connections are physically implemented.

- **Partially Parallel (PP):** Sub-units formed by sub-sets of variable and check nodes are implemented.

- **Serial (S):** Every node message is computed in order, first variable and then check.
Hardware Architecture Selection

Processing time:
HW (µs) << SW-FPGA W/R (s)

- TP
  - No Flexibility
    (no multimode)
  - X

- PP
  - X

- S
  - High Flexibility
    (allows multimode)
  - ✓
Serial architecture vs software design

Software decoding delay (1 LDPC frame) = 2.08 s

FPGA implementation of serial LDPC architecture, Toronto university:

- Throughput = 650 Mbps, clock frequency = 61 MHz
- Hardware Delay (f = 100 MHz, 1 LDPC frame) = 7.02 µs
- W/R delay = 0.19 s
- Total delay ≈ 0.2 s → 90.3% Delay Reduction
Syndrome Computation Block

- 1 1-bit comparator
- 1 inverter
- 1 Multiplier (matrix x vector)
Syndrome Computation Block

- “Efficient Hardware Design for Implementation of Matrix Multiplication by using PPI-SO”.

- 2013, Shivangi Tiwari, Nitin Meena. Dept. of EC, IES College of Technology, India.

- Higher throughput rate, 30 % less energy y 70 % less area than similar existing designs.
Syndrome Computation Block

Design for n = 3
Conclusions

- The general structure for an LDPC decoder hardware implementation was defined.

- 3 sub-blocks were designed and functionally simulated using vhdl.

- The hardware architectures for implementation of variable and check node processing and syndrome computation were selected.
Recommendations

- To implement the rest of the blocks of the LDPC decoder using the selected architectures.
- To perform functional and temporary simulations of the complete design.
5th Digital Television Forum

Hardware Implementation of Min-Sum Algorithm for LDPC Decoding

Eng. Osmanny Yaunner Núñez
MSc. Reinier Díaz Hernández
Eng. Ernesto Fontes Pupo

November, xth, 2017
DIGITAL TELEVISION LABORATORY