CABAC Decoder Hardware design and implementation with embedded system

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Introduction

- Cuba is Broadcasting the Digital Television Signal
- It does not have a National Solution for this equipment
- **LACETEL** researchers are designing some IP modules to achieve the Technology Independence
Topics

1. **Scope**: Problematic Situation, Problem, Goal, Hypothesis.

2. **Design**: CABAC overview, Hardware Solution & Software Solution in embedded system on Viterx-5 board.

3. **Results**: Time evaluation, Video Quality estimation.

4. **Conclusions and Recommendations**
Topics

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4. **Conclusions and Recommendations**
Problematic Situation (1/3)

- Compact Flash Memory
- Virtex-5 Board
- FPGA
- Power PC
- Embedded Peripherals
- Timer Ctrl
- UART Ctrl
- IT Ctrl
- Data Memory
- Program Memory
- DDR-2 Memory
Problematic Situation (2/3)

- FPGA

NO REAL TIME

- JM18.4 H.264 Reference Software
- Data Memory
- Program Memory

Embedded Peripherals
- Timer Ctrl
- UART Ctrl
- IT Ctrl

Compact Flash Memory

Virtex-5 Board

DDR-2 Memory
Problematic Situation (3/3)

Video 1
Baseline@2.0, 176x144

Video 2
Main@3.0, 352x288

Video 3
Main@3.0, 720x480

Video 4
High@4.0, 1280x720

Video 5
High@4.0, 1920x1080
H.264 overview

Data Bitstream: (0010111011011001011011010000111011301101111011101)
(120, 0), (10, 0), (8, 0), (2, 3), (-1, 2), END
## Entropy Decoding overview in H.264

### Entropy Decoder

<table>
<thead>
<tr>
<th>Syntax</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exp-Golomb</td>
<td>For others syntaxes elements such as prediction mode and QP (Quantization Parameter)</td>
</tr>
<tr>
<td>CAVLC</td>
<td>To produce quantized coefficients array in Baseline Profile</td>
</tr>
<tr>
<td>CABAC</td>
<td>To produce quantized coefficients array in others Profiles</td>
</tr>
</tbody>
</table>
Goal

Replace the **CABAC** code functions in reference code JM 19.0 for **CABAC Core IP Module**
Hypothesis

If the CABAC code functions are replaced by CABAC IP Modules (VHDL implementation) it is possible to decrease decoding time.
Topics

**Scope**: Problematic Situation, Problem, Goal, Hypothesis.

**Design**: CABAC overview, Hardware Solution & Software Solution in embedded system on Viterx-5 board.

**Results**: Time evaluation, Video Quality estimation.

**Conclusions and Recommendations**
if (A == B)
{
    X = A;
}
else
{
    X = A + B;
}
Y = FindTable[X];
## Hardware Design (3/6)

<table>
<thead>
<tr>
<th>Control Parameter</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>Rst</td>
</tr>
<tr>
<td>Start</td>
<td>Inicio</td>
</tr>
<tr>
<td>Next Bytes from Bitstream</td>
<td>Dos_Bytes</td>
</tr>
<tr>
<td>Ready</td>
<td>Fin</td>
</tr>
</tbody>
</table>

![Diagram showing control parameters and their corresponding values]
**Control Signal**
- Reset
- Start
- Next Bytes from Bitstream
- Ready

**Name**
- Rst
- Inicio
- Dos_Bytes
- Fin

**Diagram**
- MUX
- Register
- State Machine

**Input Signals**
- A
- B
- X
- Y
- Clk

**Output Signals**
- Rst
- Inicio
- Fin

**MUX Input**
- 0000000
- 1110001
- 1010010
- 0011010
- 11111111
- 0110101
- 0011110
- 1111010
- 11101010
## Hardware Design (5/6)

<table>
<thead>
<tr>
<th>Write Signal</th>
<th>bits</th>
<th>Write Signal</th>
<th>bits</th>
<th>Read Signal</th>
<th>bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>codeILow</td>
<td>32</td>
<td>Syntax Element</td>
<td>6</td>
<td>Symbol</td>
<td>32</td>
</tr>
<tr>
<td>Descript</td>
<td>4</td>
<td>Dos Bytes</td>
<td>16</td>
<td>Next Bytes</td>
<td>1</td>
</tr>
<tr>
<td>QP</td>
<td>6</td>
<td>Inicio</td>
<td>1</td>
<td>Fin</td>
<td>1</td>
</tr>
</tbody>
</table>

### Write Registers

- **0**:
  - codeILow (32 bits)

- **1**: 0x00
  - Descript (4 bits)
  - QP (6 bits)
  - Syntax Element (6 bits)
  - Dos Bytes (16 bits)

### Read Register

- **2**:
  - Symbol (32 bits)
Hardware Design (6/6)

FPGA

CABAC IP Module

JM19.0 H.264 Reference Software

Data Memory Program Memory

Timer Ctrl UART Ctrl IT Ctrl

Embedded Peripherals

Compact Flash Memory

DDR-2 Memory

Virtex-5 Board
Topics

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4. Conclusions and Recommendations
Time analysis of system (1/4)

PC
JM 19.0

Set parameters
Profile
Level
Bit Rate
...

Video Input with YUV format

Video Output With .264 format
# Time analysis of system (2/4)

<table>
<thead>
<tr>
<th>H.264 Video (Bit rate)</th>
<th>Resolution</th>
<th>Profile@Level</th>
<th>Entropy Decoder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video 1 (Low)</td>
<td>176 x 144</td>
<td>Baseline@2.0</td>
<td>CAVLC</td>
</tr>
<tr>
<td>Video 2 (Low)</td>
<td>352 x 288</td>
<td>Main@3.0</td>
<td></td>
</tr>
<tr>
<td>Video 3 (Average)</td>
<td>720 x 480</td>
<td>Main@3.0</td>
<td>CABAC</td>
</tr>
<tr>
<td>Video 4 (Average)</td>
<td>1280x720</td>
<td>High@4.0</td>
<td></td>
</tr>
<tr>
<td>Video 5 (High)</td>
<td>1920x1080</td>
<td>High@4.0</td>
<td></td>
</tr>
</tbody>
</table>
Time analysis of system (3/4)

Compact Flash

Virtex-5 FPGA

PowerPC 440

... 

CABAC {

Timer start

... 

Read timer

... 

Decompressed Video

PLB Bus

INTC

TIMER

CABAC DECODER
**Time analysis of system (4/4)**

*Time of videos 1.0s*

*Result of 15 Experiments*

*Average Values with error < 0.1s*

*Decrease decoding time in 98% respect to software solution*
Time analysis of system (3/4)

- Compact Flash
- PowerPC 440
  - Timer start
  - ... 
  - ... 
  - ... 
  - Read timer
- Virtex-5 FPGA
- Compressed Video
- Decompressed Video
- PLB Bus
- Decompressed Video
- CABAC DECODER
- TIMER
- INTC
Time analysis of system (4/4)

Time of videos 1.0s

Result of 15 Experiments

Average Values with error < 0.1s

Decrease decoding time in 18% - 19% respect to software solution

Dec. Time IP Module

Dec. Time JM 19.0

18% - 19%

CAVLC

TIME (s)

Video 1

Video 2

Video 3

Video 4

Video 5
Video Quality Estimation (1/4)

A: Original Video
B: Decoded Video

DMOS
(Diferencia de la puntuación de opinión media)
# Video Quality Estimation (1/4)

<table>
<thead>
<tr>
<th>H.264 Video (Bit rate)</th>
<th>Resolution</th>
<th>Profile@Level</th>
<th>Bit Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video 1 (Low)</td>
<td>720 x 480</td>
<td>Main@3.0</td>
<td>1.8Mbps</td>
</tr>
<tr>
<td>Video 2 (Low)</td>
<td>720 x 480</td>
<td>Main@3.0</td>
<td>1.8Mbps</td>
</tr>
<tr>
<td>Video 3 (Average)</td>
<td>1920x1080</td>
<td>High@4.0</td>
<td>4.9Mbps</td>
</tr>
<tr>
<td>Video 4 (Average)</td>
<td>1920x1080</td>
<td>High@4.0</td>
<td>4.9Mbps</td>
</tr>
<tr>
<td>Video 5 (High)</td>
<td>1920x1080</td>
<td>High@4.0</td>
<td>4.9Mbps</td>
</tr>
</tbody>
</table>
Time analysis of system (4/4)

Result of 15 Experiments

Average Values

Rec. ITU-R BT 1203-2

DMOS (%)

With IP module

Software JM19.0

1920x1080

4.9Mbps
**Time analysis of system (4/4)**

**Result of 15 Experiments**

**Average Values**

- With IP module
- Software JM19.0

**Rec. ITU-R BT 1203-2**

- 720x480
- 1.8Mbps
**Result of 15 Experiments**

**Average Values**

<table>
<thead>
<tr>
<th>Bitrate (Mbps)</th>
<th>DMOS (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>3.5</td>
<td></td>
</tr>
</tbody>
</table>

*With IP module* vs *Software JM19.0*

Video 5
720x480

*Rec. ITU-R BT 1203-2*
Topics


2. Design: CABAC overview, Hardware Solution & Software Solution in embedded system on Viterx-5 board.

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Conclusions

• The CABAC Decoder was designed as IP module and it reduce decoding delay at least 98% respect to software (JM 19.0) solution.

• The IP module and fitted into the main H.264/AVC decoder system and it reduce decoding delay at least 18%.

• In videos with HD configurations, the video quality is according to Rec. ITU-R BT.1203-2.

• In videos with SD configurations, the video quality is according to Rec. ITU-R BT.1203-2 when bitrate is higher than 3.0Mbps.
Recommendations

• To design all modules with signals 0 to Length-1.
• To design the *Inverse Scan* block in next time.
Hardware design and implementation of the CABAC Decoder with embedded system

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