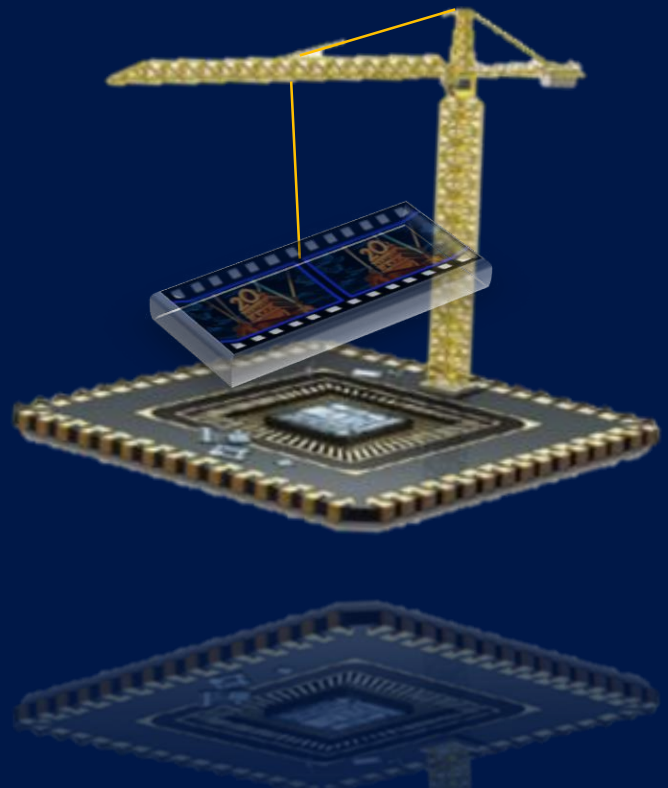
RESEARCH & DEVELOPMENT TELECOMMUNICATION'S INSTITUTE

CABAC Decoder Hardware design and implementation with embedded system



Authors:

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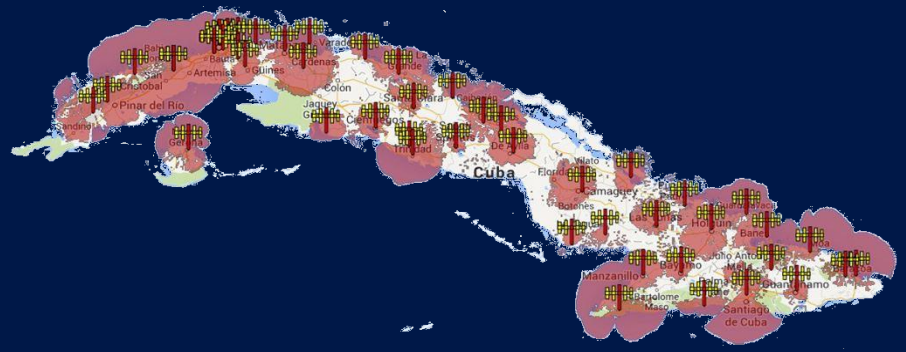
Eng. Gustavo Aguirre Soler

Havana, November 2017

Introduction



- Cuba is Broadcasting the Digital Television Signal
- It does not have a National Solution for this equipment
- ***LACETEL*** researchers are designing some IP modules to achieve the Technology Independence

DTMB Modulat IP Modu

Data-bro EPG DVB Subtitle

H.264 Decoder IP Module

Topics

1. **Scope:** Problematic Situation, Problem, Goal, Hypothesis.
2. **Design:** CABAC overview, Hardware Solution & Software Solution in embedded system on Viterx-5 board.
3. **Results:** Time evaluation, Video Quality estimation.
4. **Conclusions and Recommendations**

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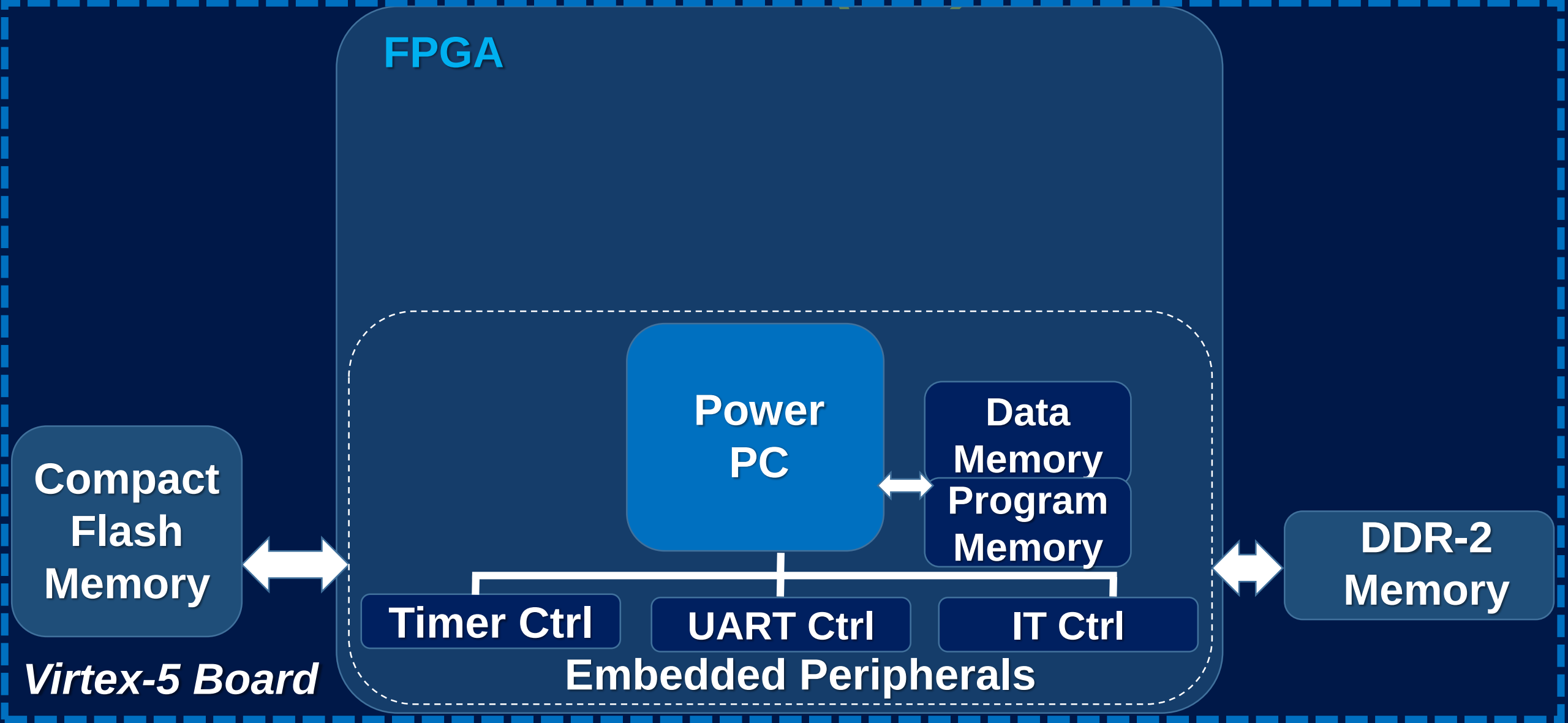
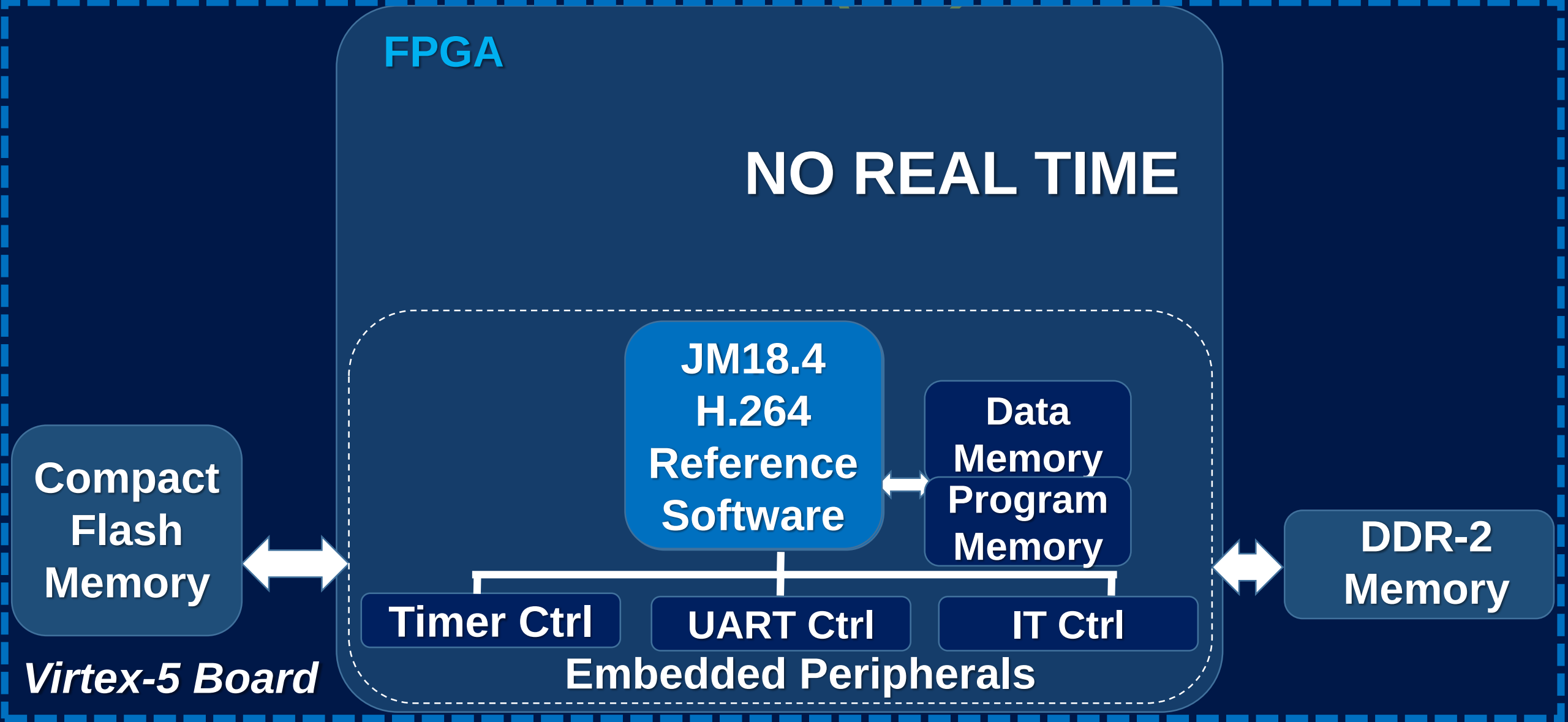
Problematic Situation (1/3)

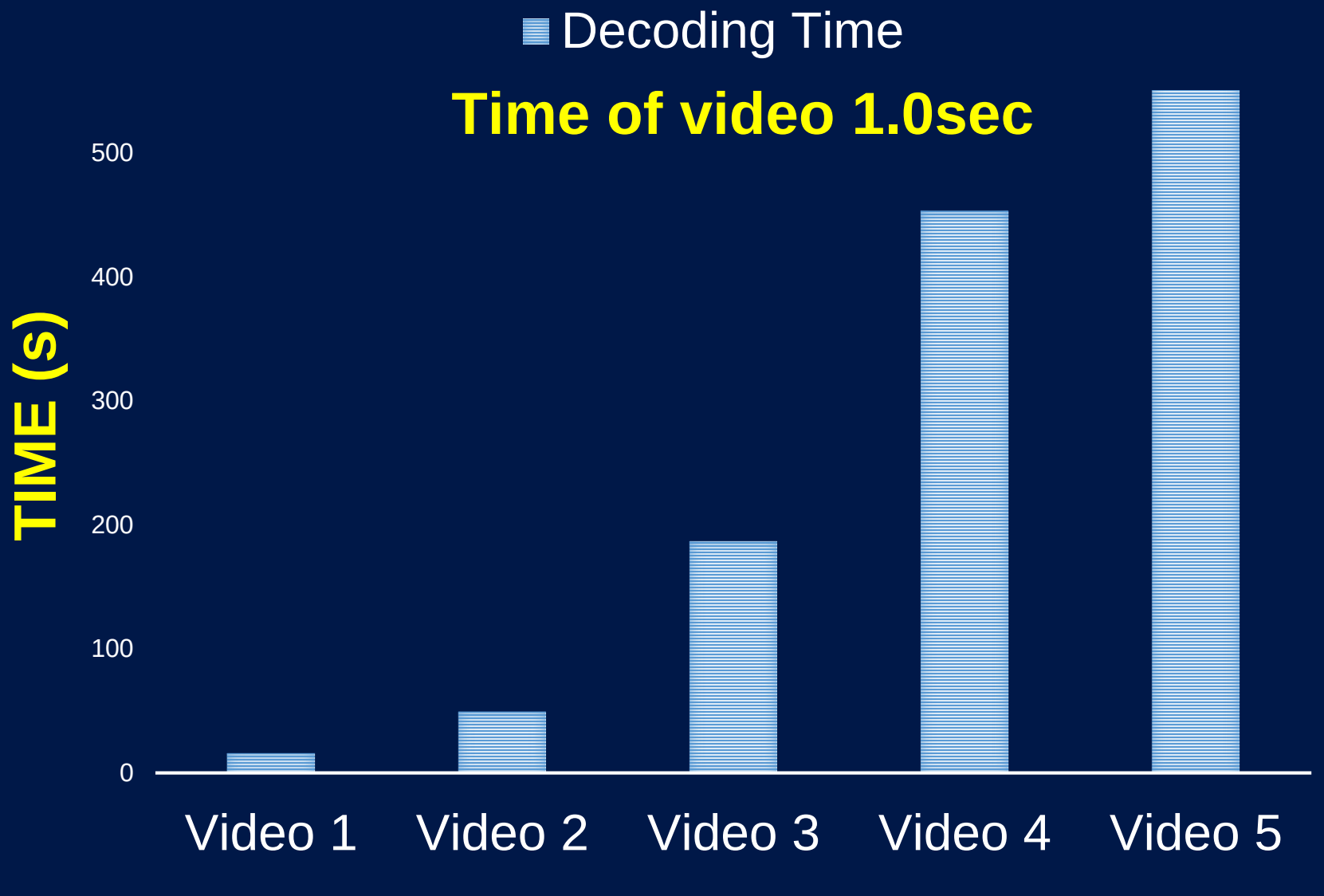


Problematic Situation (2/3)

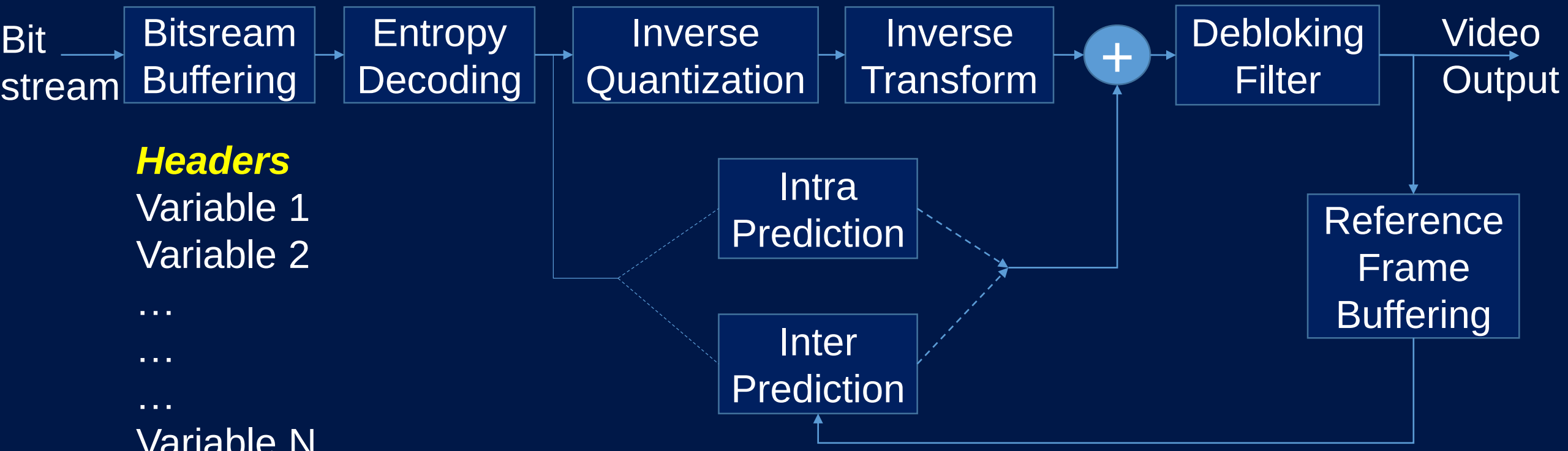


Problematic Situation (3/3)

Video 1
Baseline@2.0, 176x144
Video 2
Main@3.0, 352x288
Video 3
Main@3.0, 720x480
Video 4
High@4.0, 1280x720
Video 5
High@4.0, 1920x1080



H.264 overview



Headers

Variable 1

Variable 2

…

…

…

Variable N

…

Data Bitstream (0010111011011001010111010000111010110110011110110)

(120, 0), (10, 0), (8, 0), (2, 3), (-1, 2), END

Entropy Decoding overview in H.264

Entropy Decoder

Exp-Golomb	For others syntaxes elements such as prediction mode and QP (Quantization Parameter)
CAVLC	To produce quantized coefficients array in Baseline Profile
CABAC	To produce quantized coefficients array in others Profiles

Goal

Replace the ***CABAC*** code functions in reference code JM 19.0 for ***CABAC Core*** IP Module

Hypothesis

If the CABAC code functions are replaced by CABAC IP Modules (VHDL implementation) it is possible to decrease decoding time.

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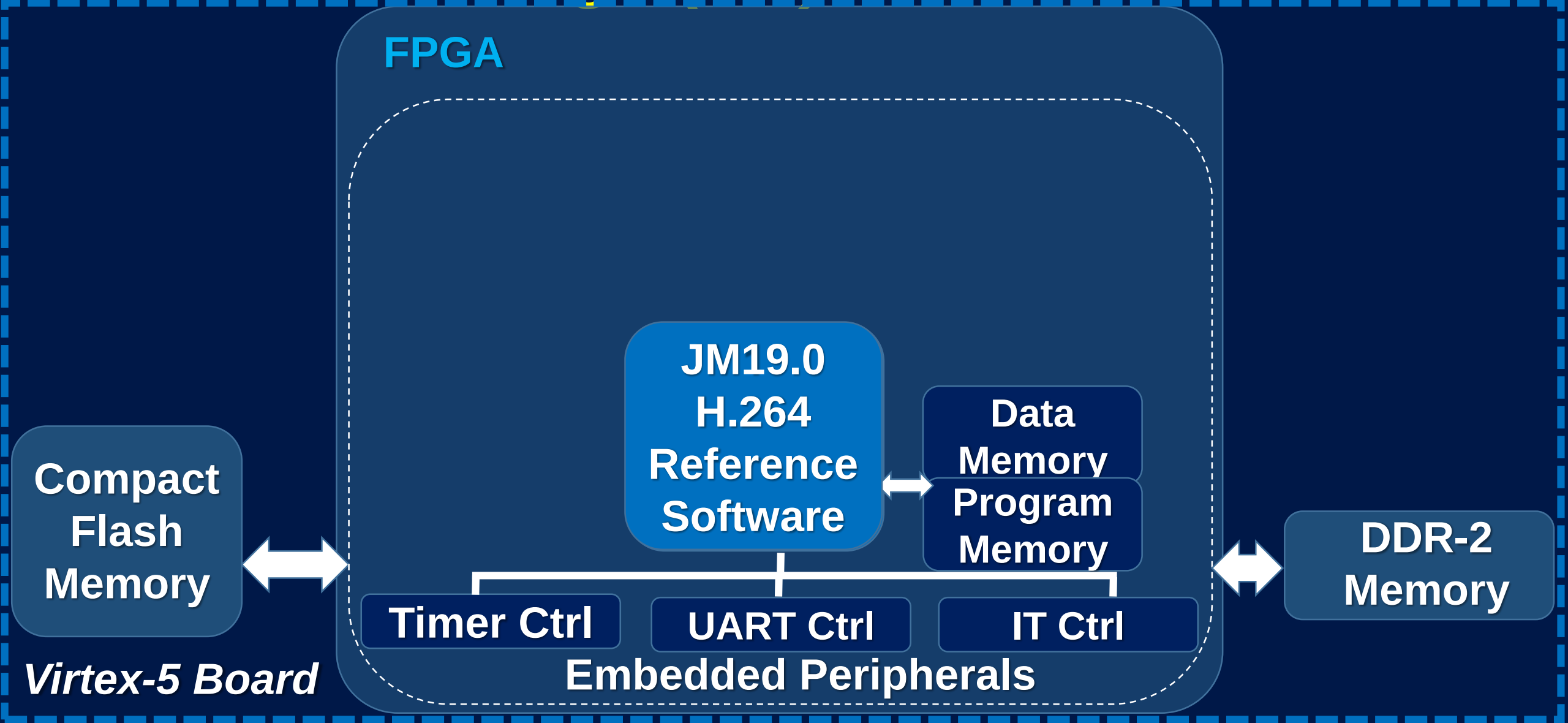
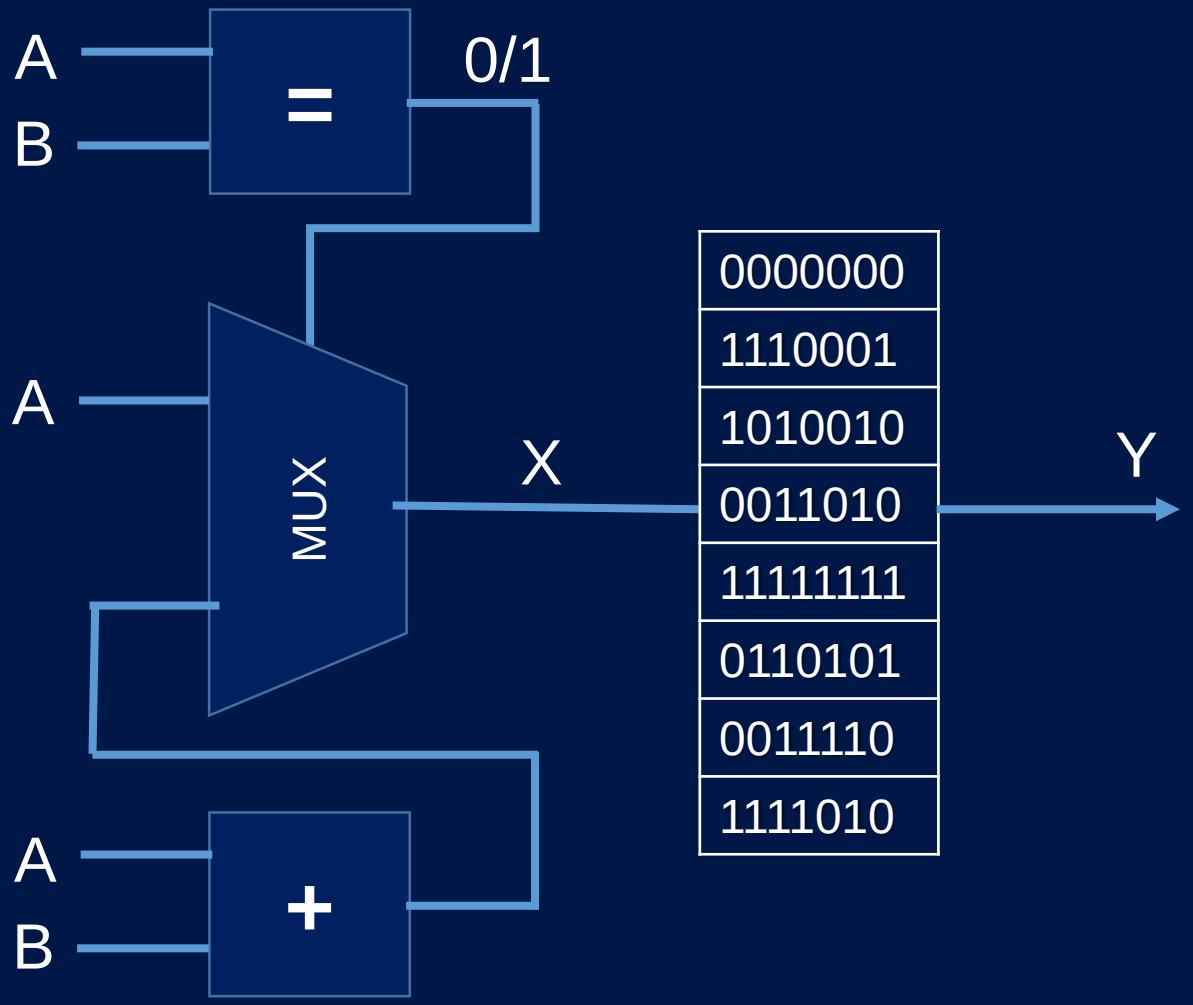
Hardware Design (1/6)



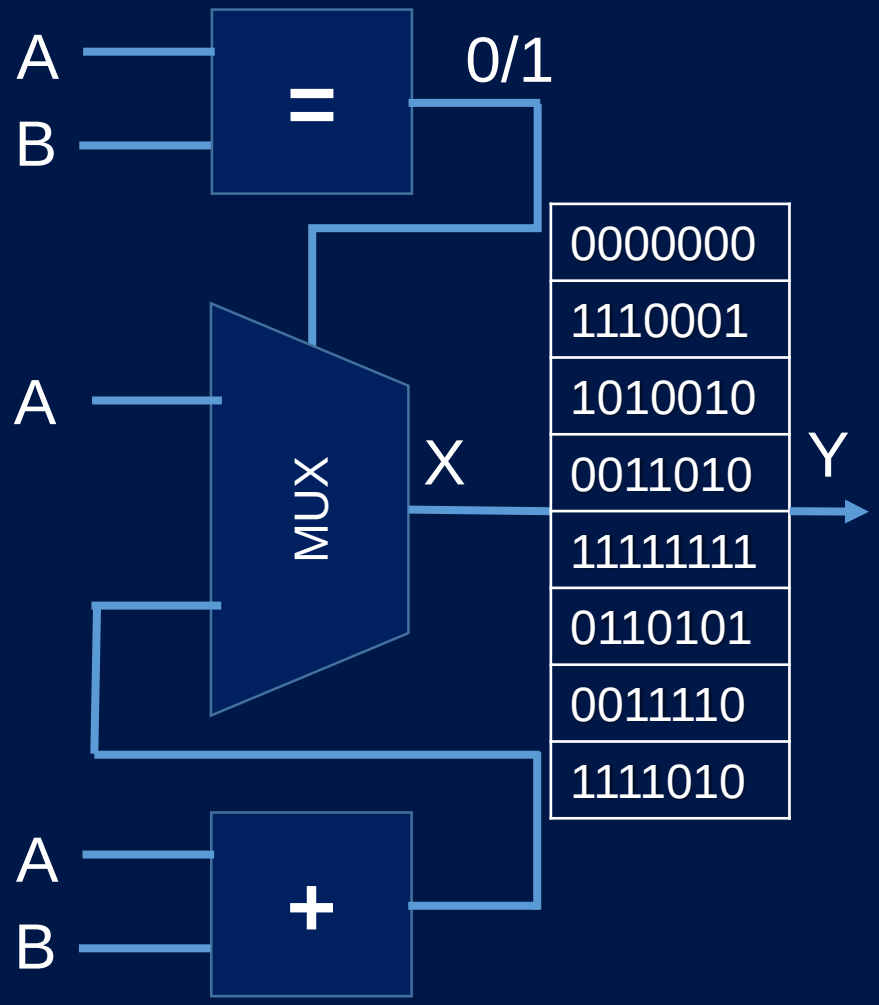
Hardware Design (2/6)

```
if (A == B)
{
  X= A;
}
else
{
  X= A+B;
}
Y = FindTable[X];
```



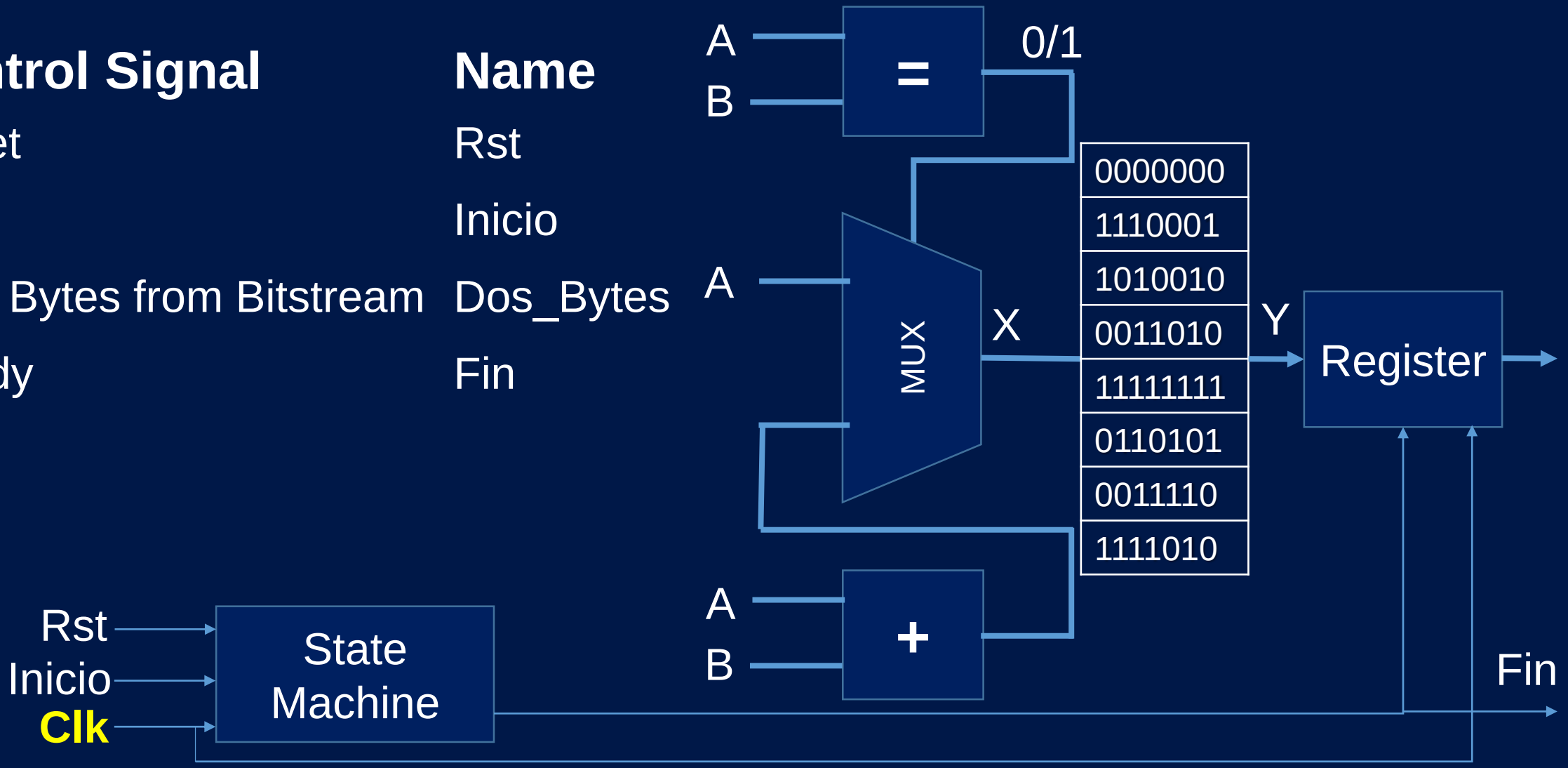
Hardware Design (3/6)

Control Parameter	Name
Reset	Rst
Start	Inicio
Next Bytes from Bitstream	Dos_Bytes
Ready	Fin



Hardware Design (4/6)

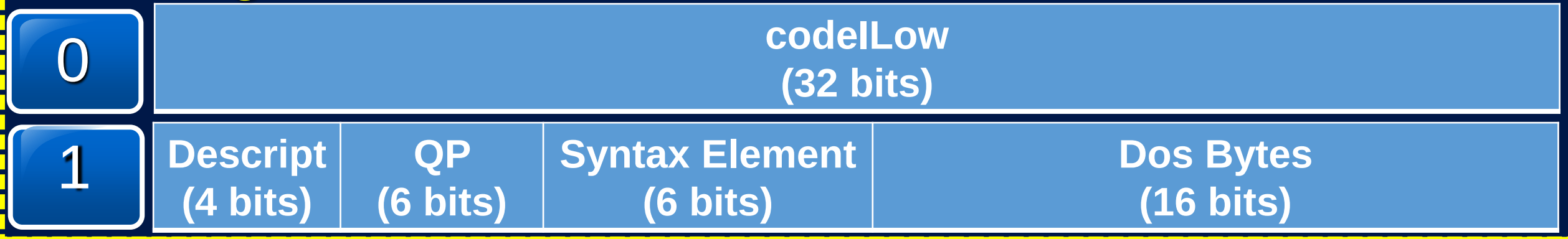
Control Signal	Name
Reset	Rst
Start	Inicio
Next Bytes from Bitstream	Dos_Bytes
Ready	Fin



Hardware Design (5/6)

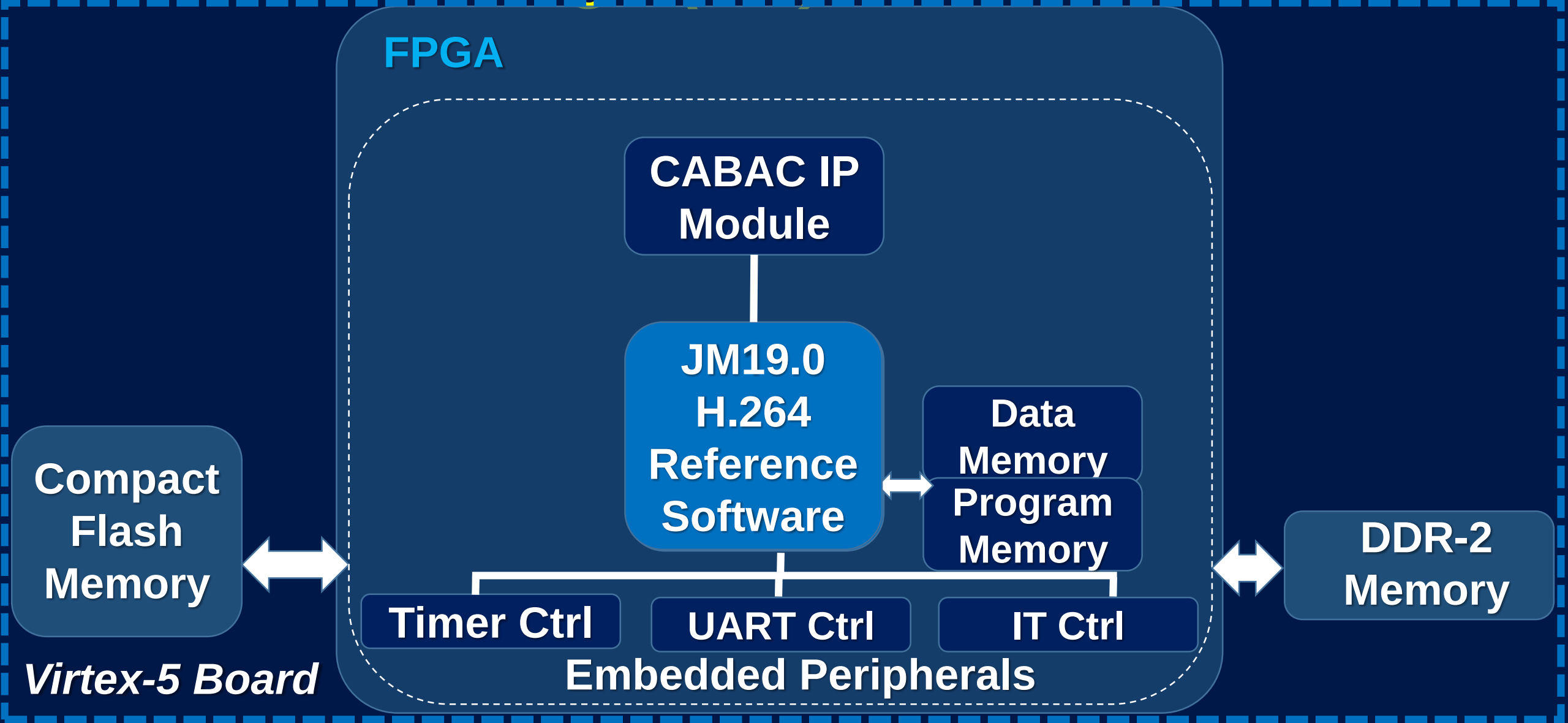
Write Signal	bits	Write Signal	bits	Read Signal	bits
codeILow	32	Syntax Element	6	Symbol	32
Descript	4	Dos Bytes	16	Next Bytes	1
QP	6	Inicio	1	Fin	1

Write Registers



Read Register

Hardware Design (6/6)



Topics

1

Scope: Problematic Situation, Problem, Goal, Hypothesis.

2

Design: CABAC overview, Hardware Solution & Software Solution in embedded system on Viterx-5 board.

3

Results: Time evaluation, Video Quality estimation.

4

Conclusions and Recommendations

Time analysis of system (1/4)

Video Input with YUV format

PC

JM 19.0

Set parameters

Profile

Level

Bit Rate

...

Microsoft® Visual Studio®

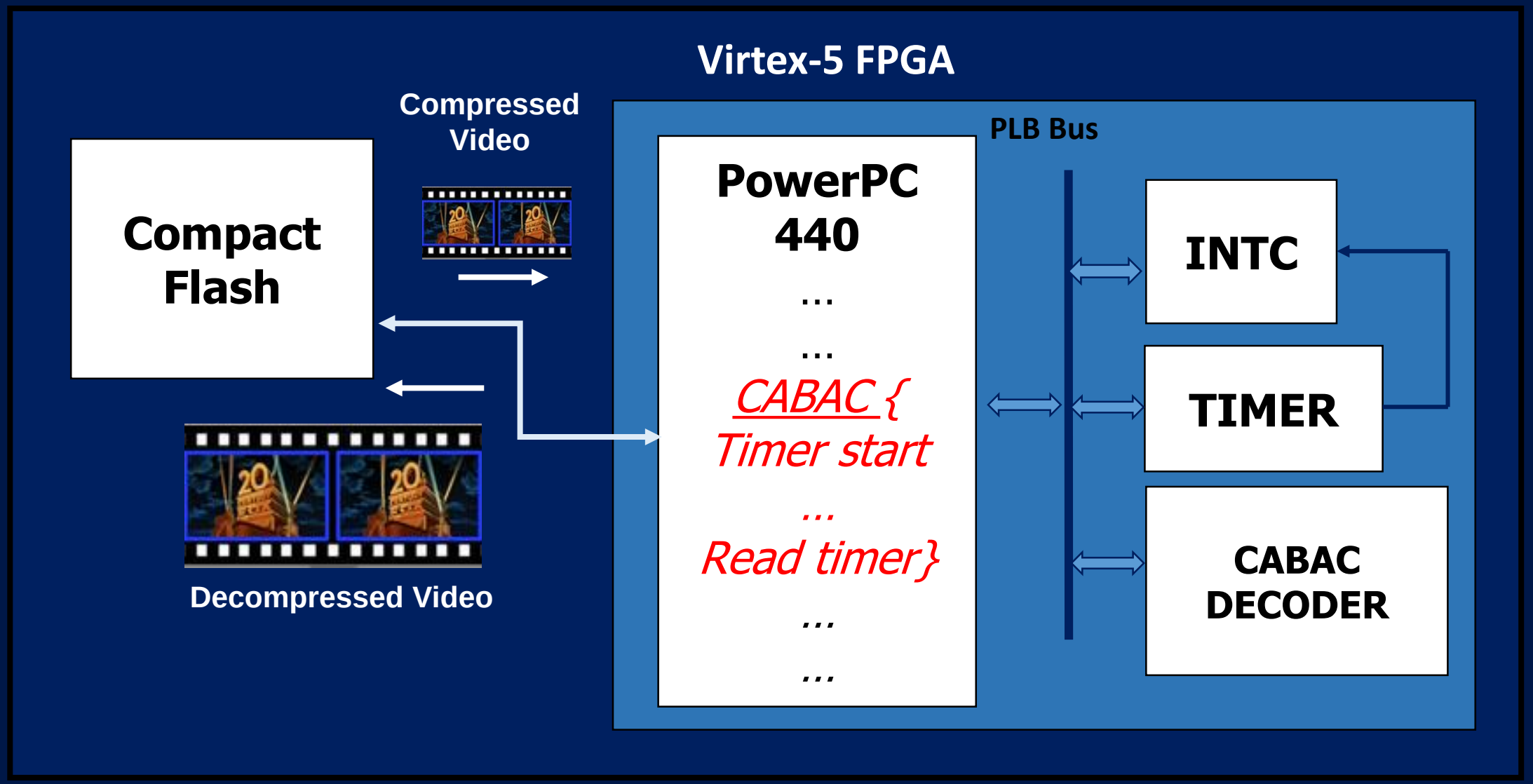
Video Output With .264 format

Time analysis of system (2/4)

H.264 Video (Bit rate)	Resolution	Profile@Level	Entropy Decoder
Video 1 (Low)	176 x 144	Baseline@2.0	CAVLC
Video 2 (Low)	352 x 288	Main@3.0	CABAC
Video 3 (Average)	720 x 480	Main@3.0	
Video 4 (Average)	1280x720	High@4.0	
Video 5 (High)	1920x1080	High@4.0	

Microsoft Visual Studio

Time analysis of system (3/4)



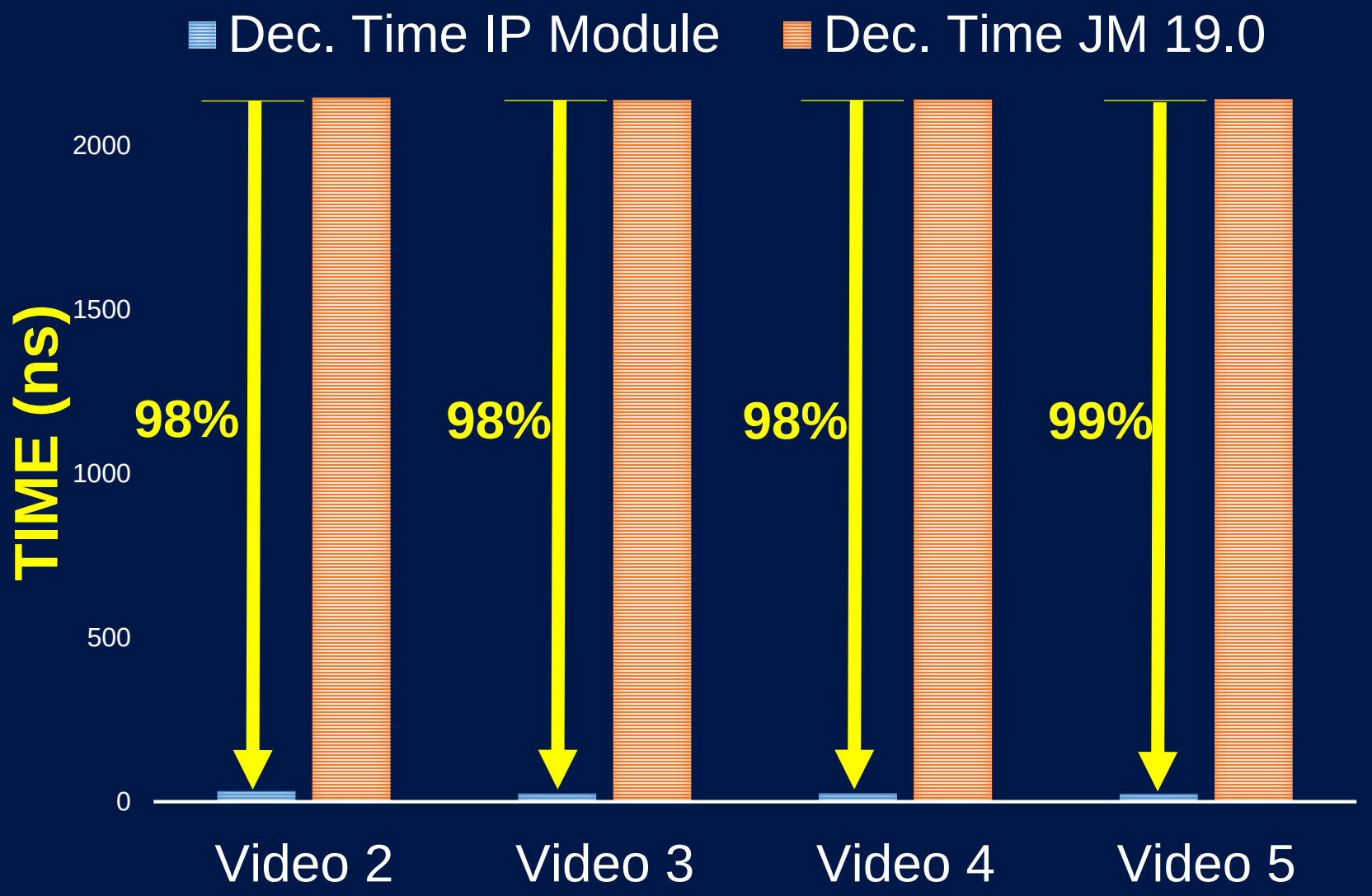
Time analysis of system (4/4)

Time of videos 1.0s

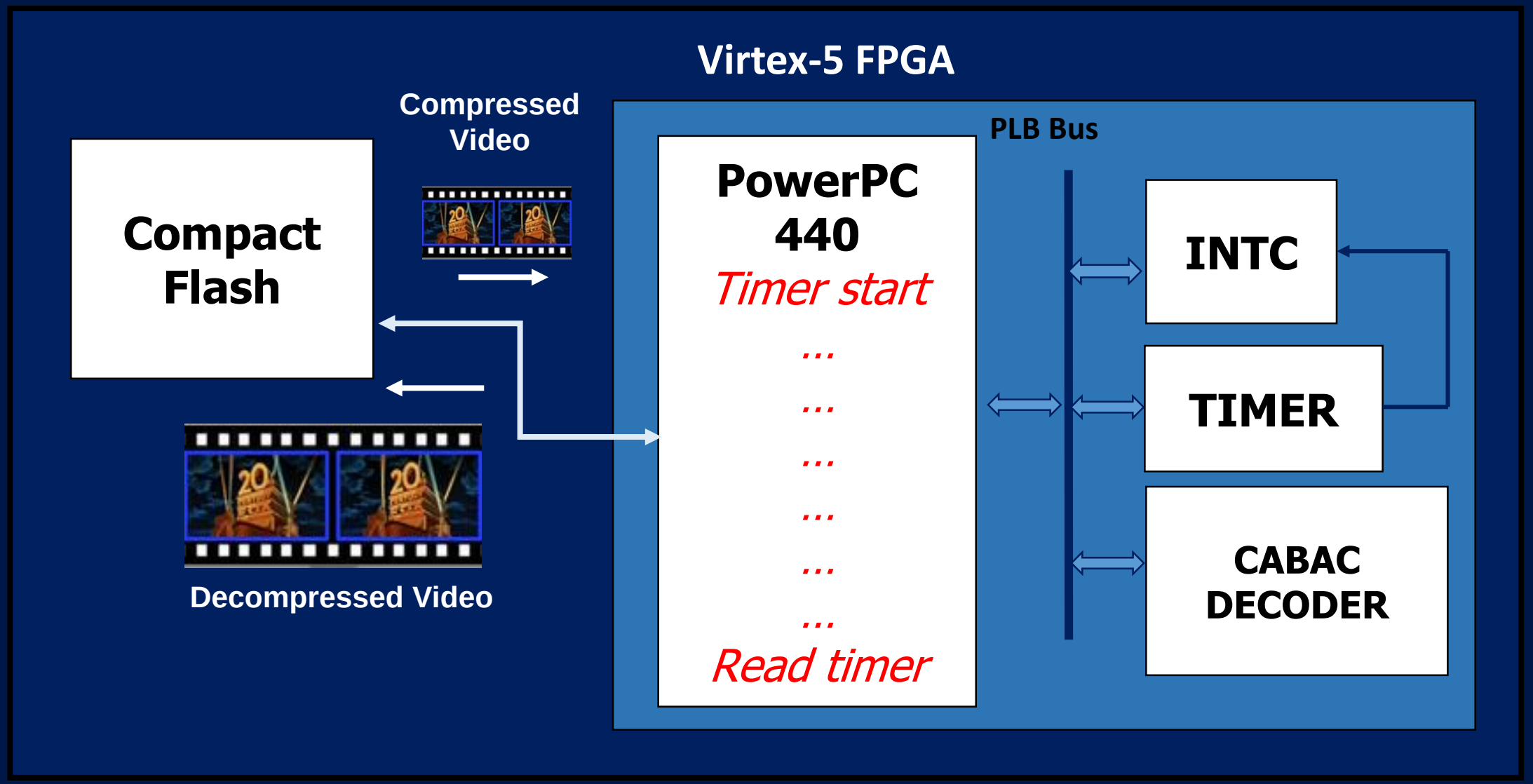
Result of 15 Experiments

Average Values with error < 0.1s

Decrease decoding time in 98% respect to software solution



Time analysis of system (3/4)



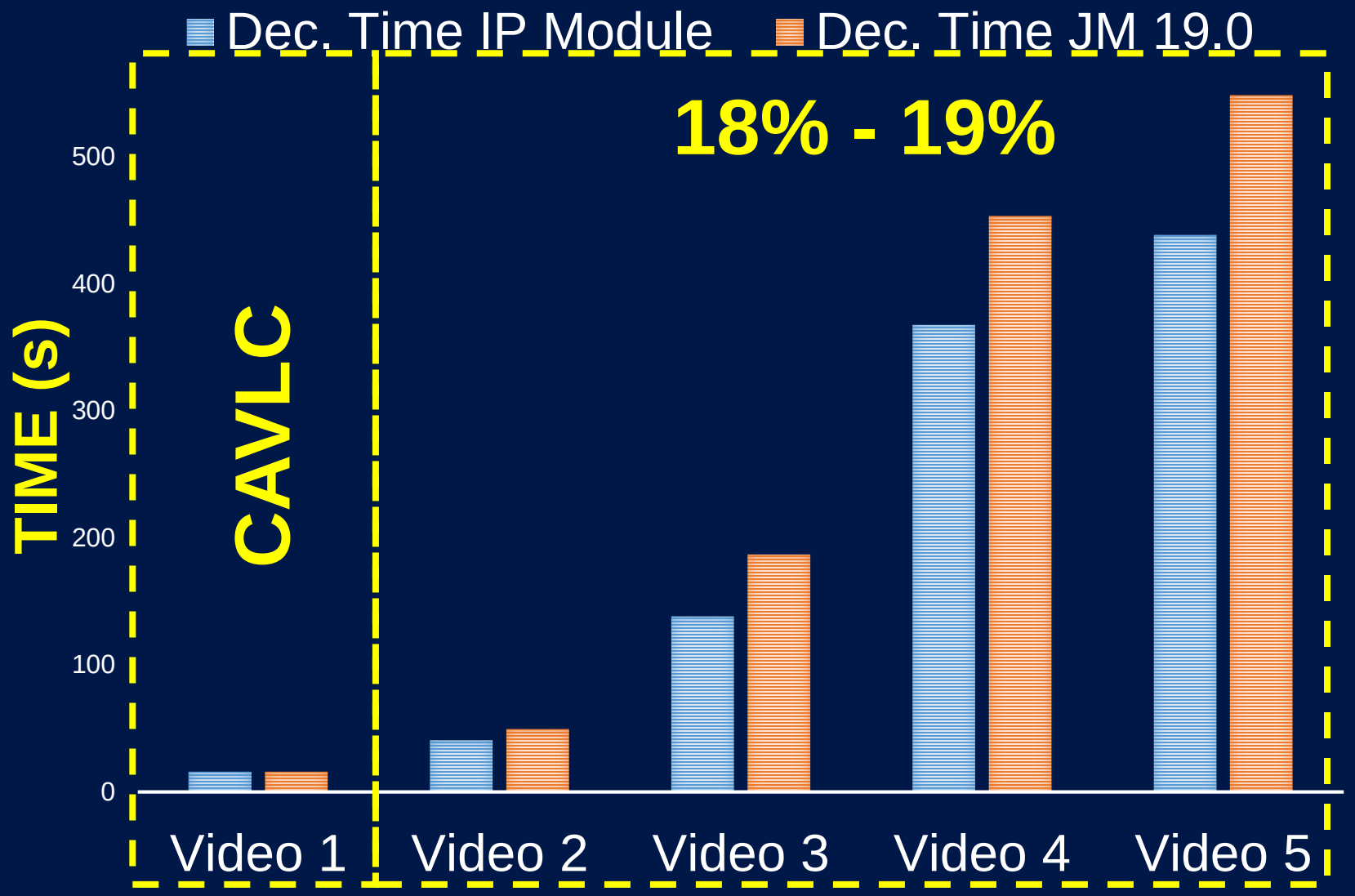
Time analysis of system (4/4)

Time of videos 1.0s

Result of 15 Experiments

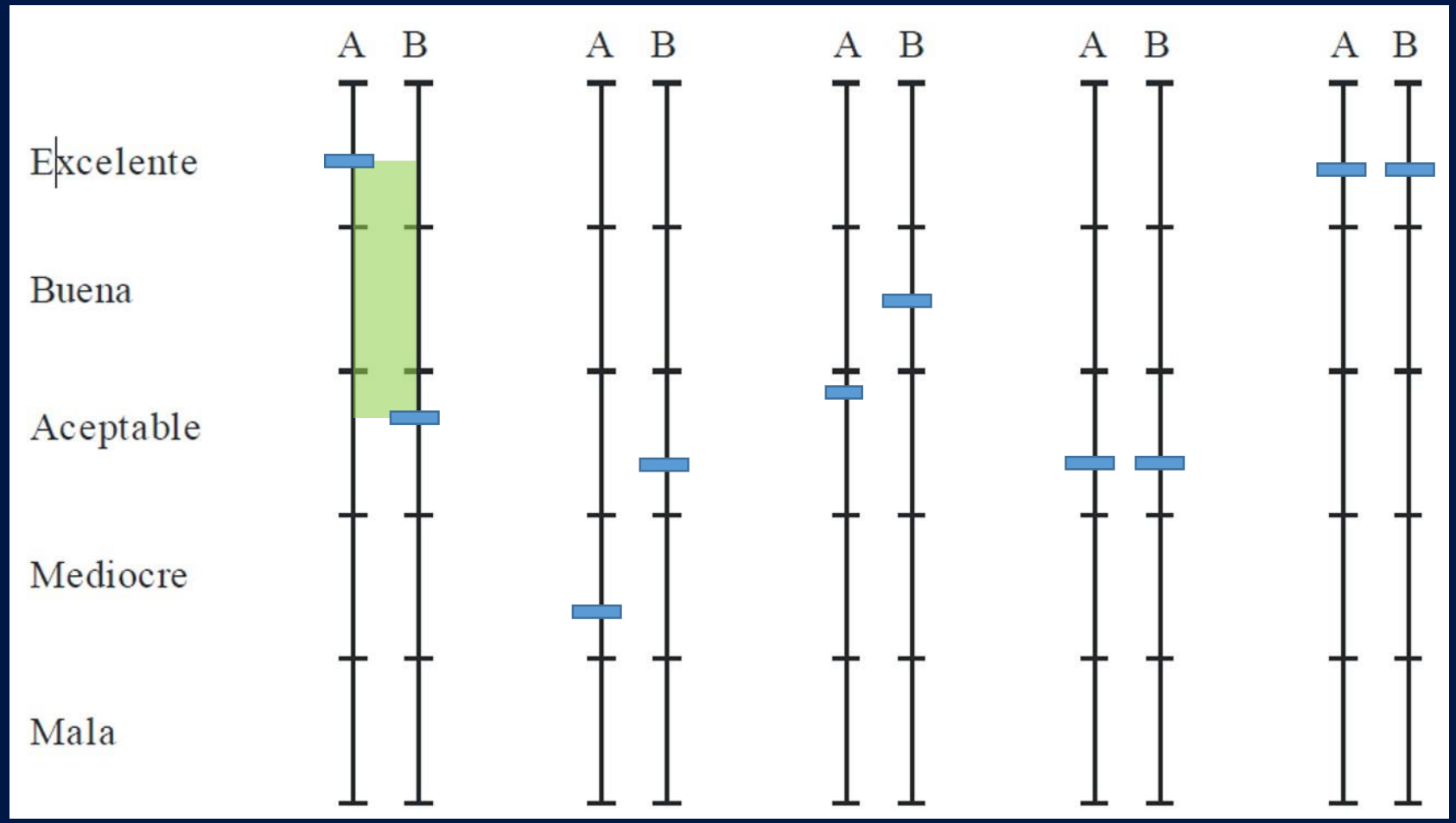
Average Values with error < 0.1s

Decrease decoding time in 18% - 19% respect to software solution



Video Quality Estimation (1/4)

A: Original Video **B:** Decoded Video



DMOS

(Diferencia de la puntuación de opinión media)

Video Quality Estimation (1/4)

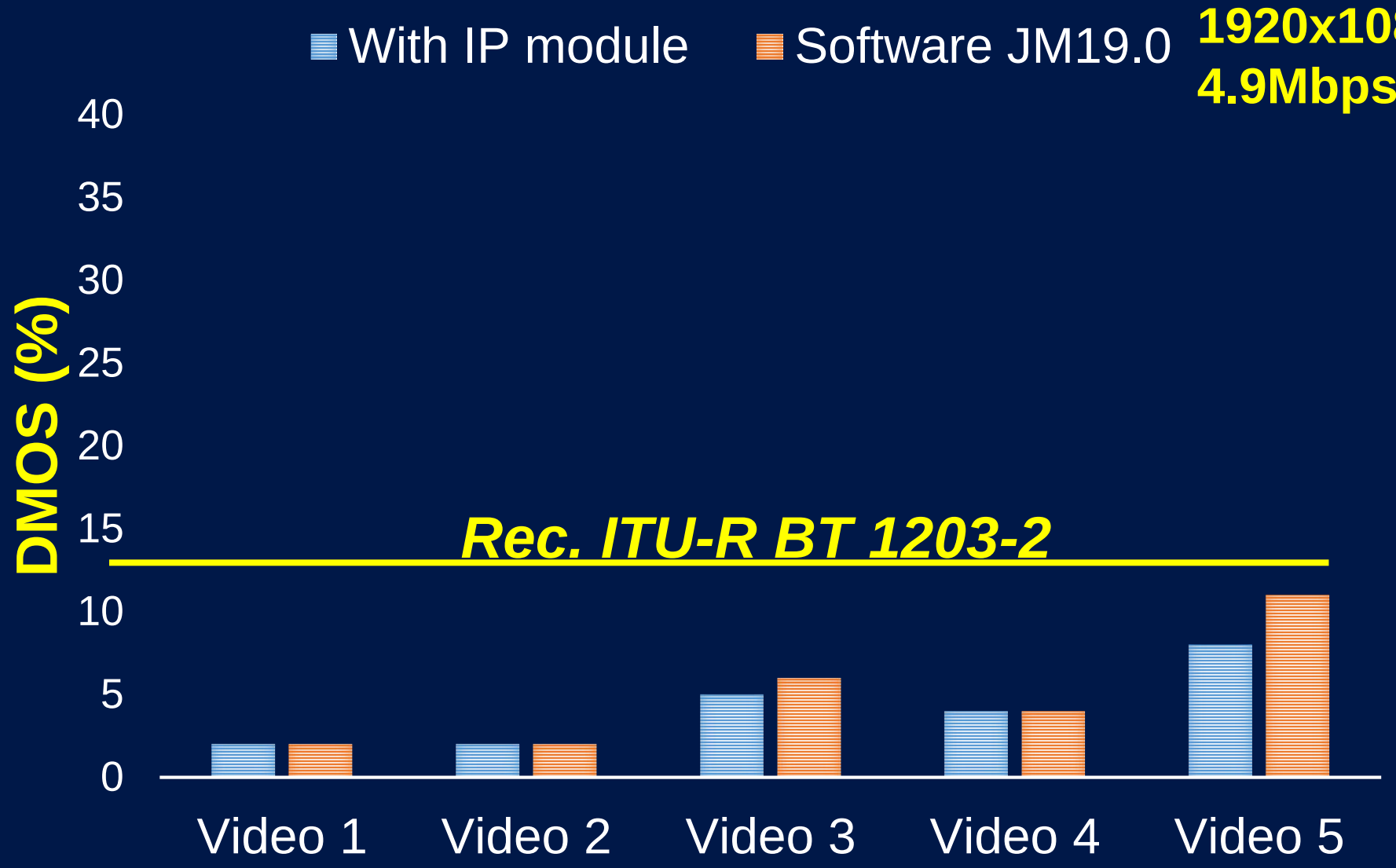
H.264 Video (Bit rate)	Resolution	Profile@Level	Bit Rate
Video 1 (Low)	720 x 480 1920x1080	Main@3.0 High@4.0	1.8Mbps 4.9Mbps
Video 2 (Low)			
Video 3 (Average)			
Video 4 (Average)			
Video 5 (High)			

Microsoft Visual Studio

Time analysis of system (4/4)

Result of 15 Experiments

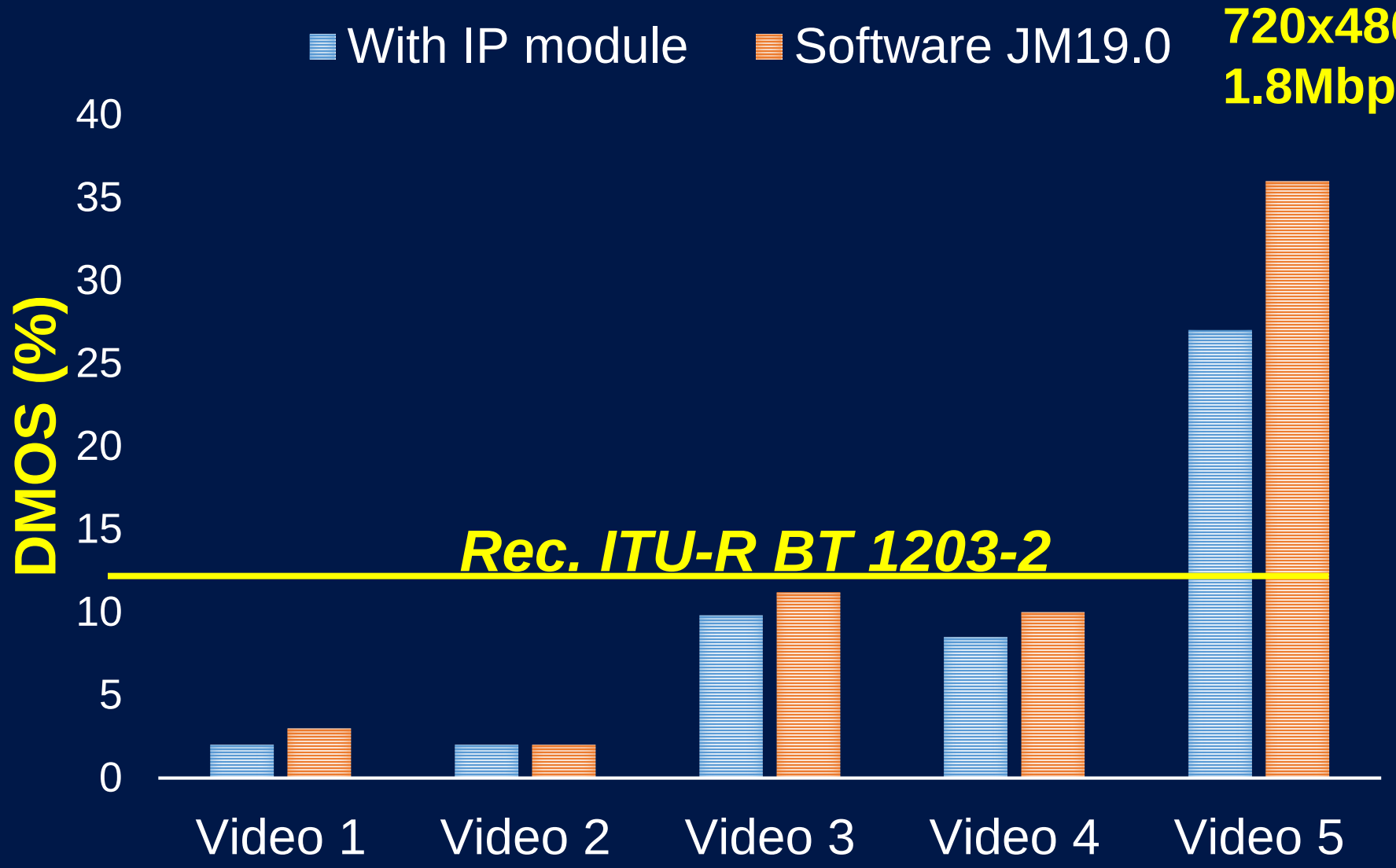
Average Values



Time analysis of system (4/4)

Result of 15 Experiments

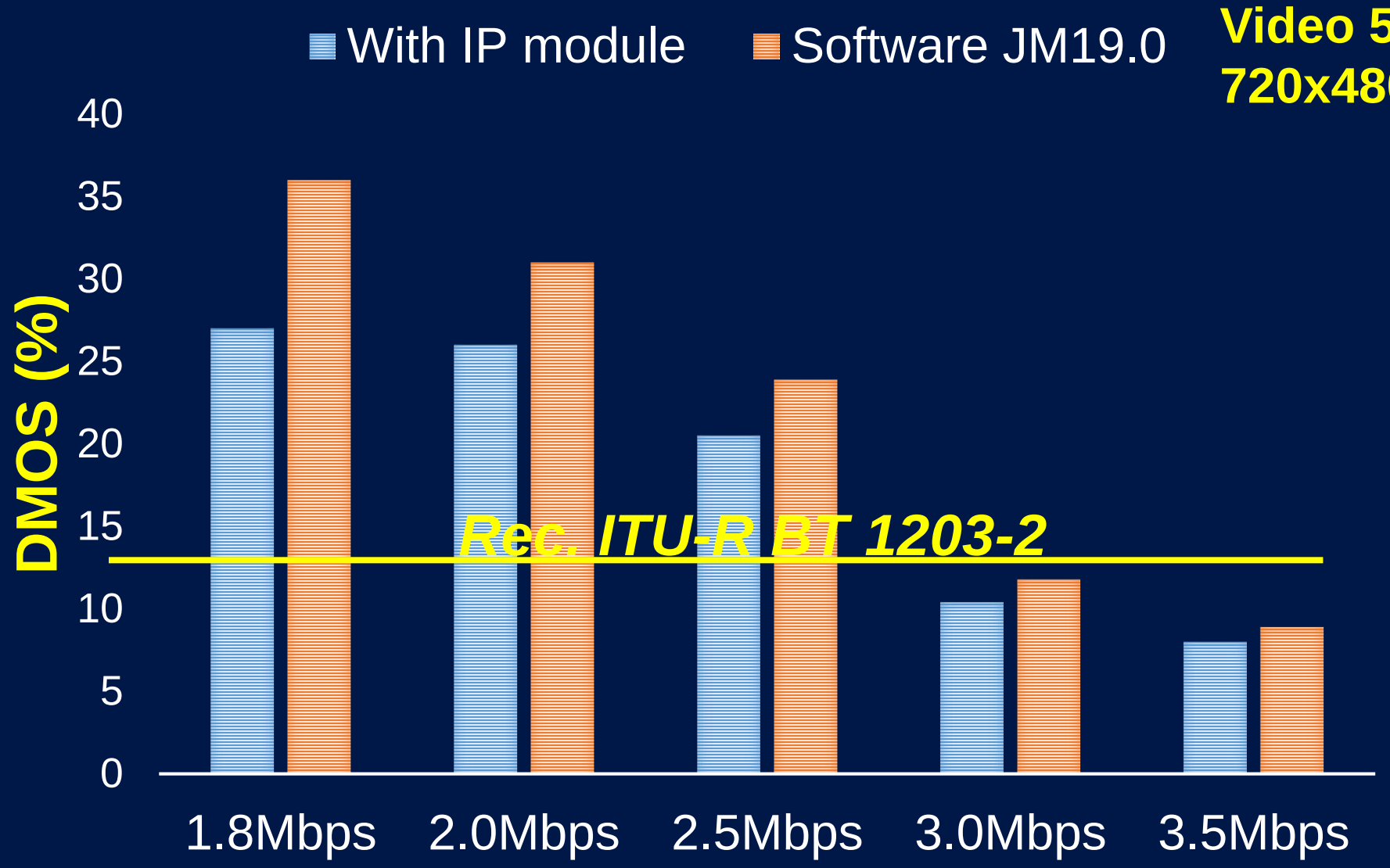
Average Values



Time analysis of system (4/4)

Result of 15 Experiments

Average Values



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Conclusions

- The CABAC Decoder was designed as IP module and it reduce decoding delay at least 98% respect to software (JM 19.0) solution.
- The IP module and fitted into the main H.264/AVC decoder system and it reduce decoding delay at least 18%.
- In videos with HD configurations, the video quality is according to Rec. ITU-R BT.1203-2.
- In videos with SD configurations, the video quality is according to Rec. ITU-R BT.1203-2 when bitrate is higher than 3.0Mbps.

Recommendations

- To design all modules with signals 0 to Lengh-1.
- To design the *Inverse Scan* block in next time.

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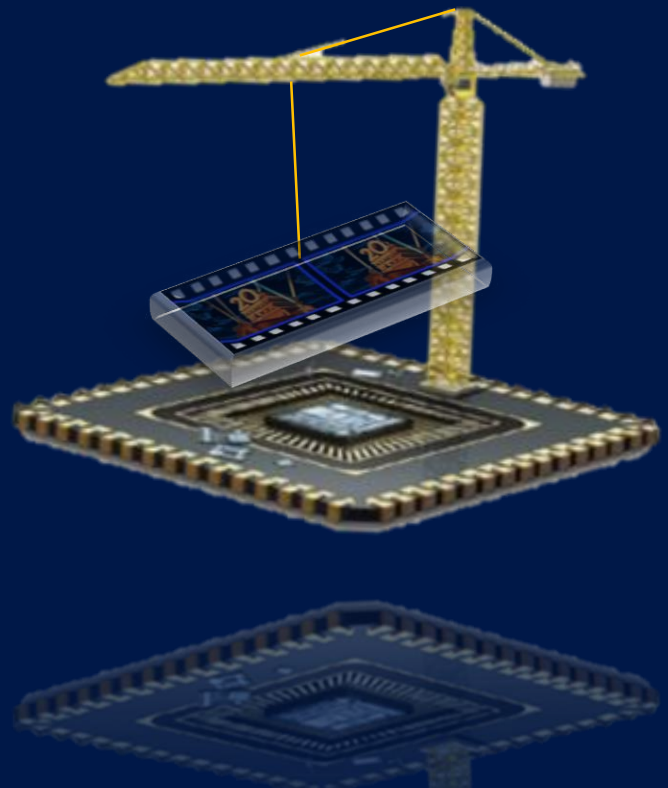
Hardware design and implementation of the CABAC Decoder with embedded system



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