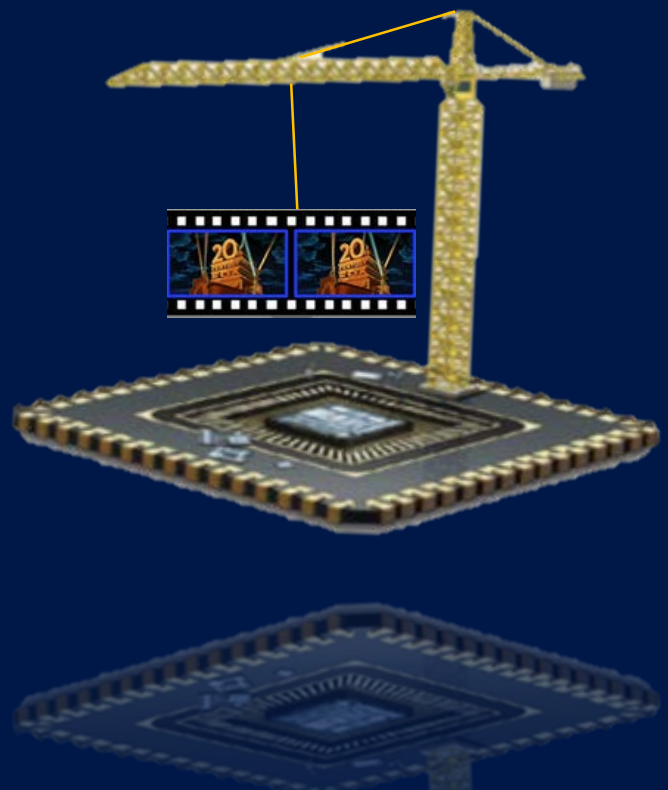
RESEARCH & DEVELOPMENT TELECOMMUNICATION'S INSTITUTE

Hardware Implementation of the H.264/AVC CABAC Entropy Decoding Core



Authors:

Eng. Rufino R. Cabrera Álvarez

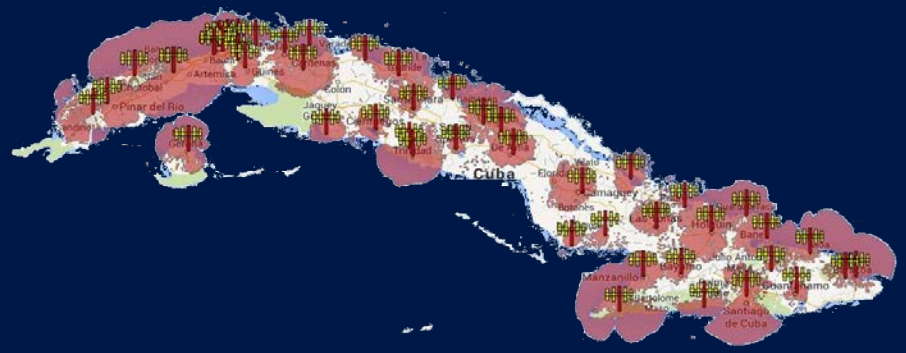
Eng. Osmany Yaunner Núñez

Eng. Orlando Landrove Gámez

PhD. Glauco Guillén Nieto

Havana, September 2015

Introduction



- Cuba is broadcasting the Digital Television Signal

- It does not have a National Solution for this equipment

- ***LACETEL*** researchers are designing some IP modules to achieve the Technology Independence

DTMB Modulat IP Modu

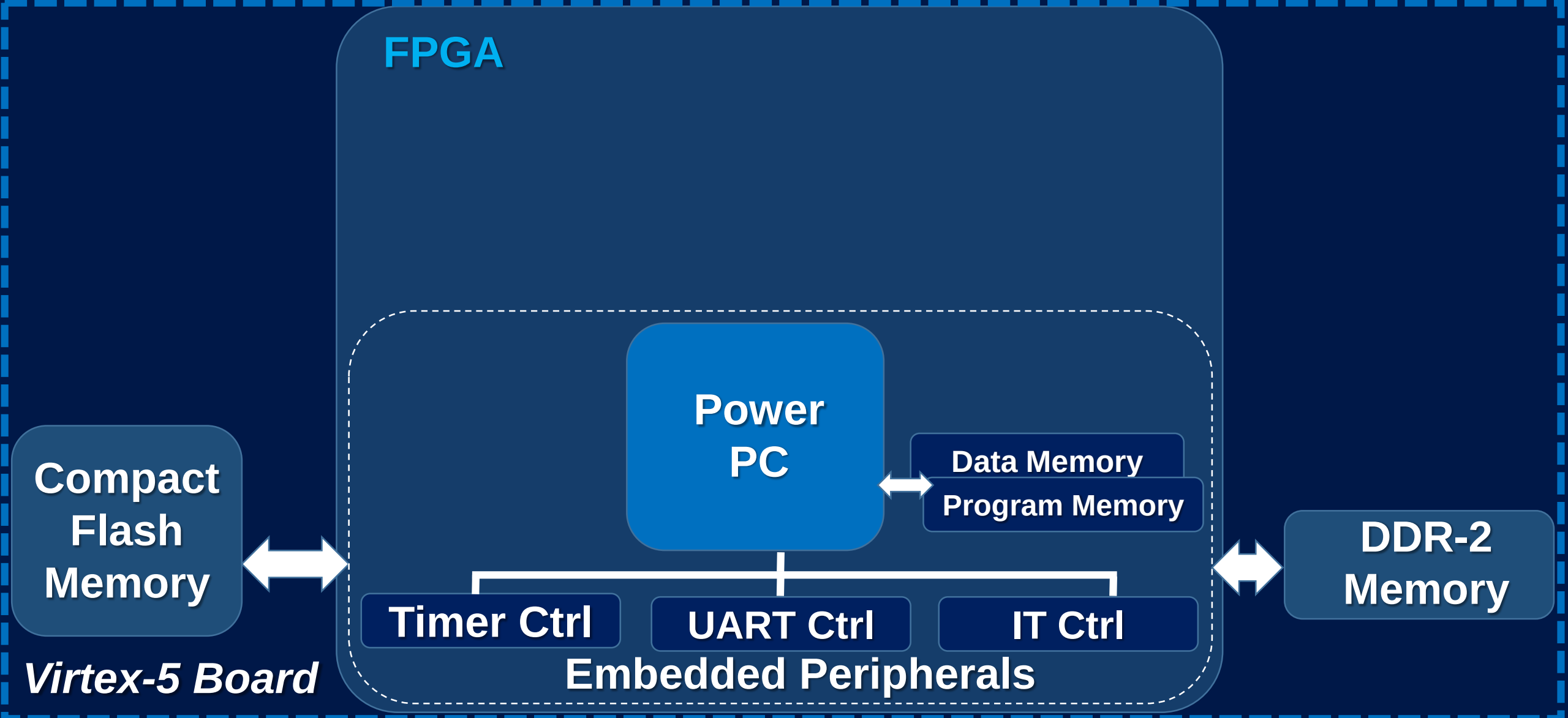
DTMI De-Modulator IP Module

H.264 Decoder IP Module

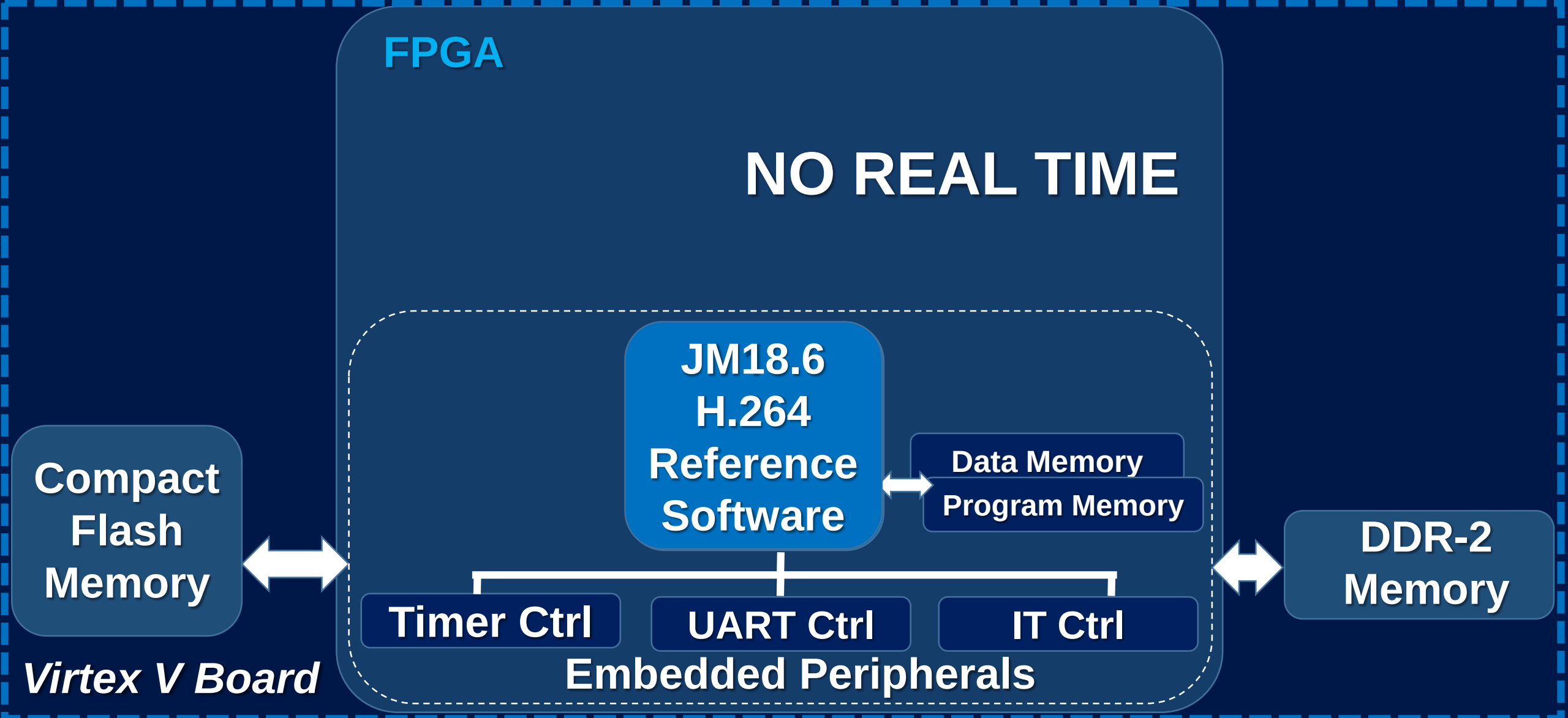
Content

Content

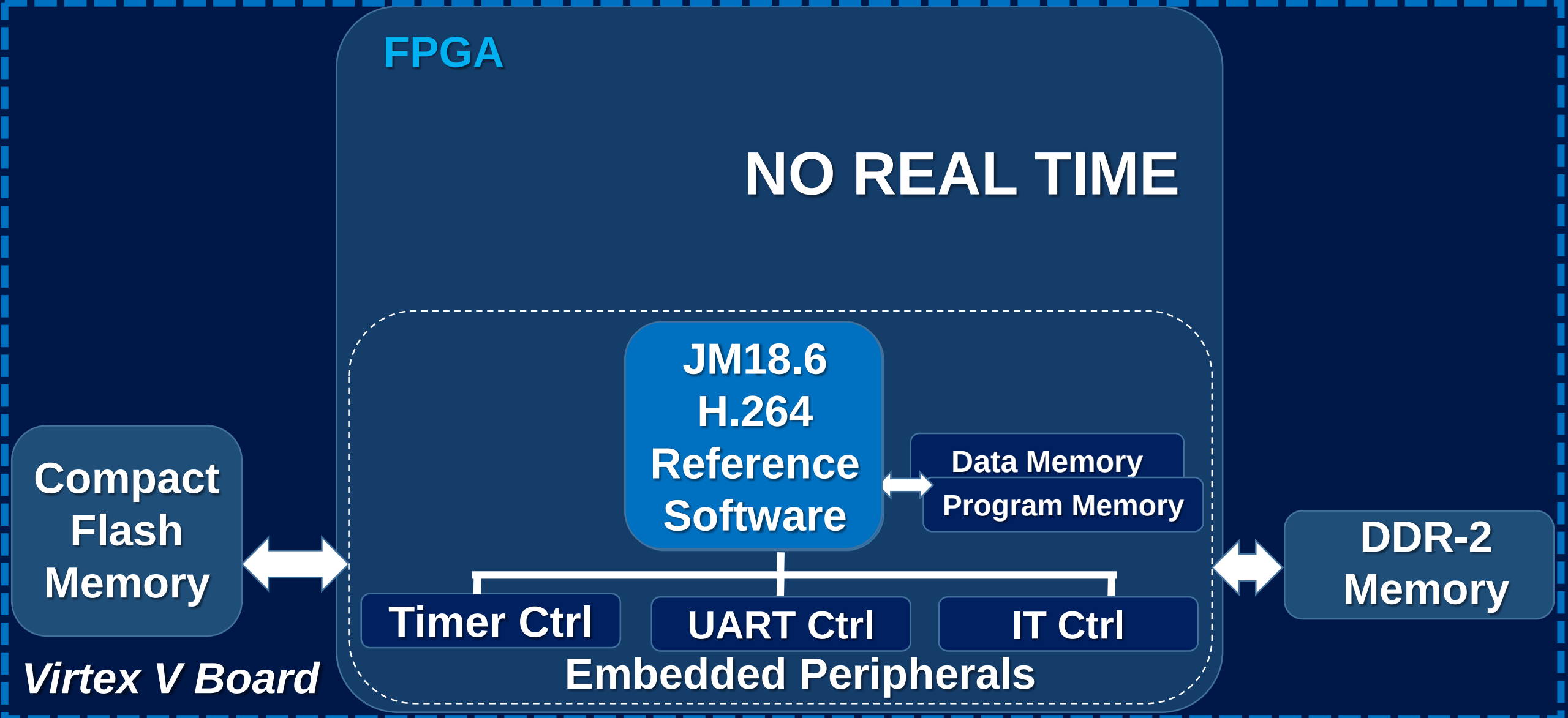
Problematic Situation



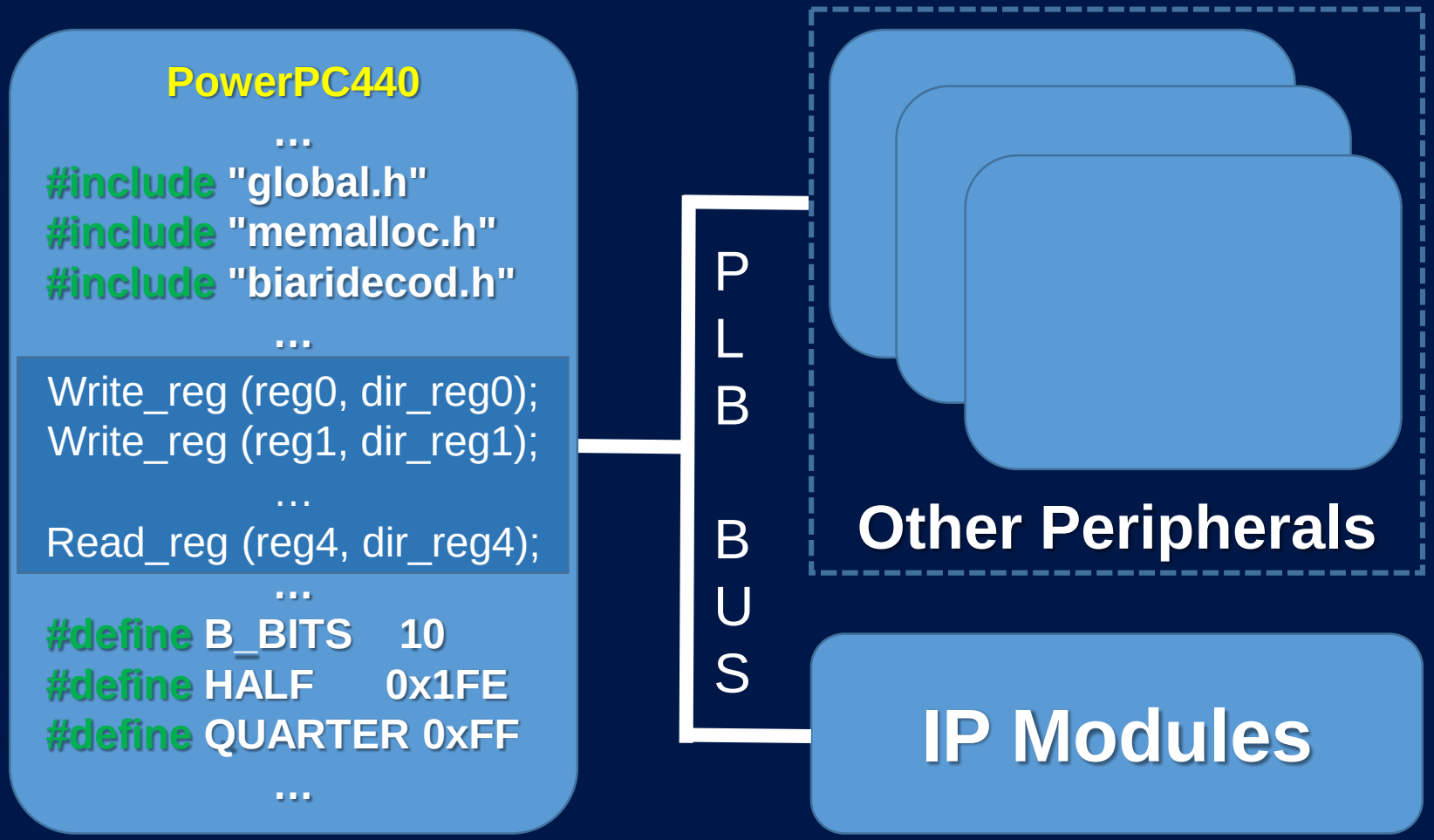
Problematic Situation



Problematic Situation

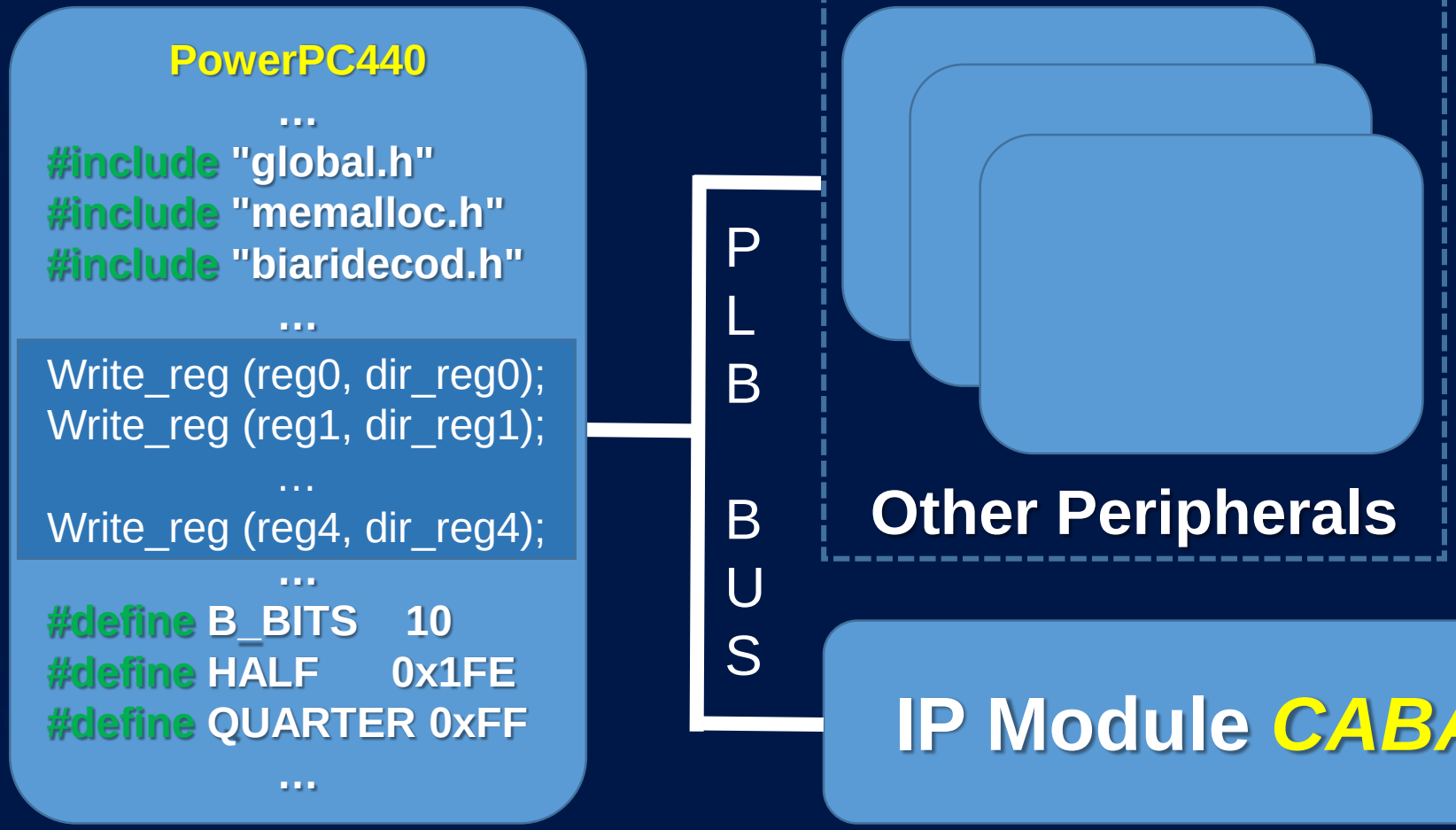


Problematic Situation



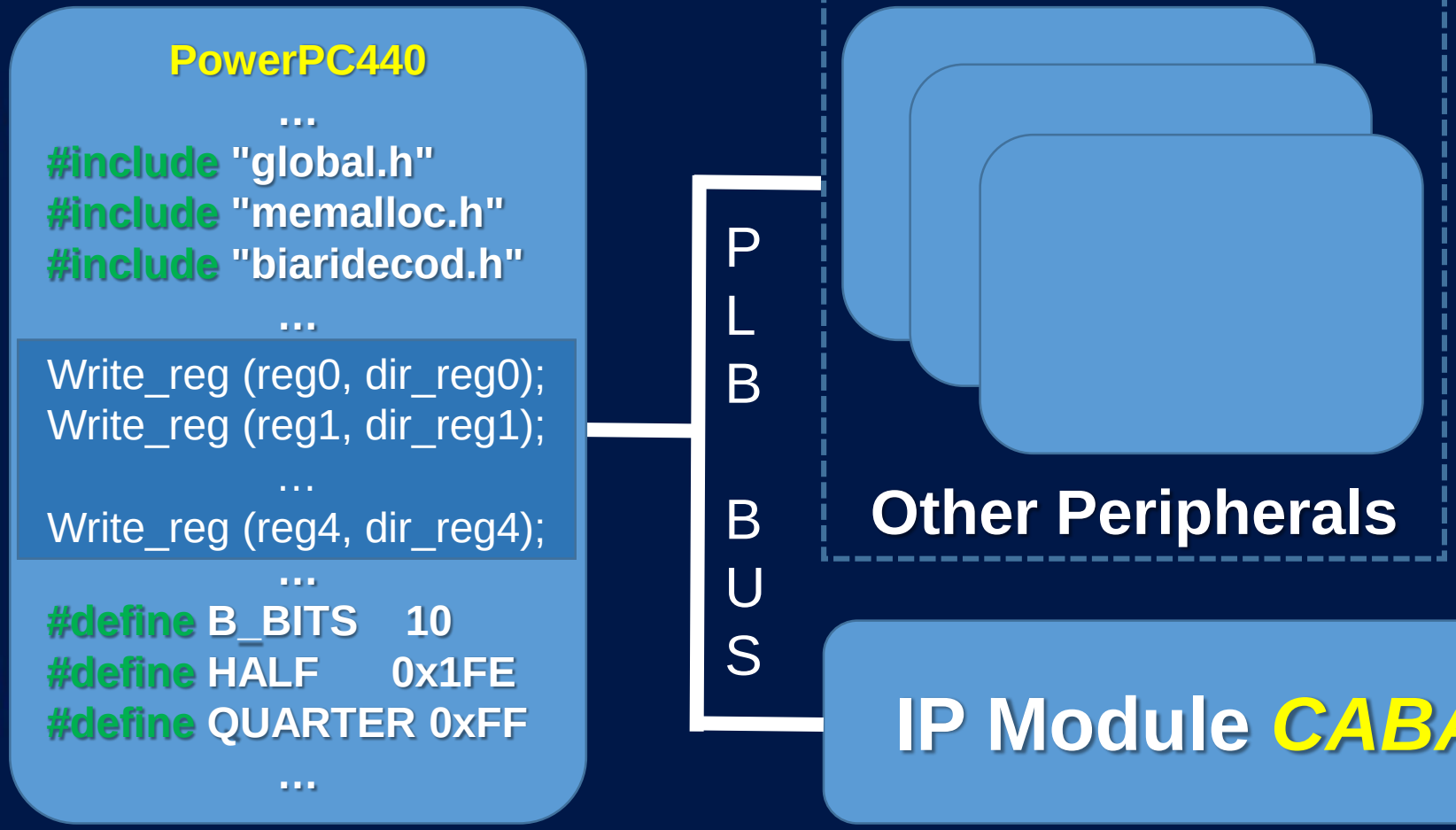
If some code functions are replaced by IP Modules (VHDL implementation) it is possible to decrease the system decoding time.

Goal



Replace the ***Arithmetic Binary Decoder*** code functions by ***CABAC Core*** IP Module

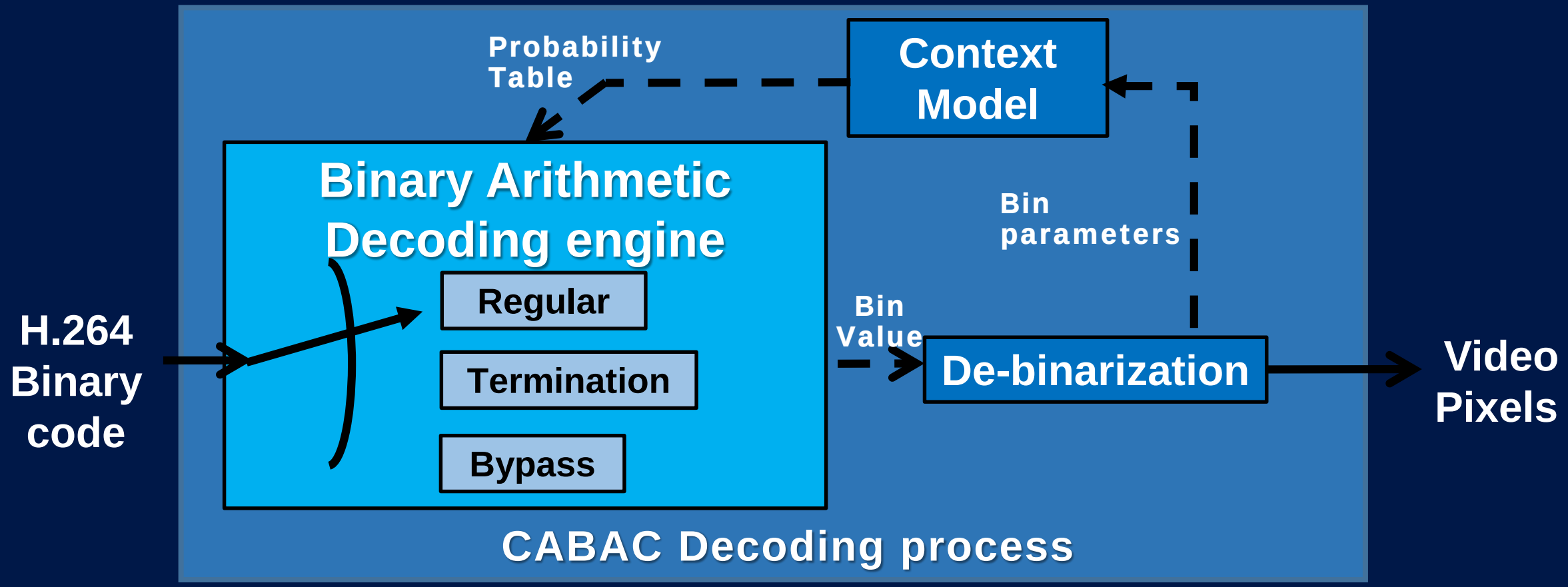
Hypothesis



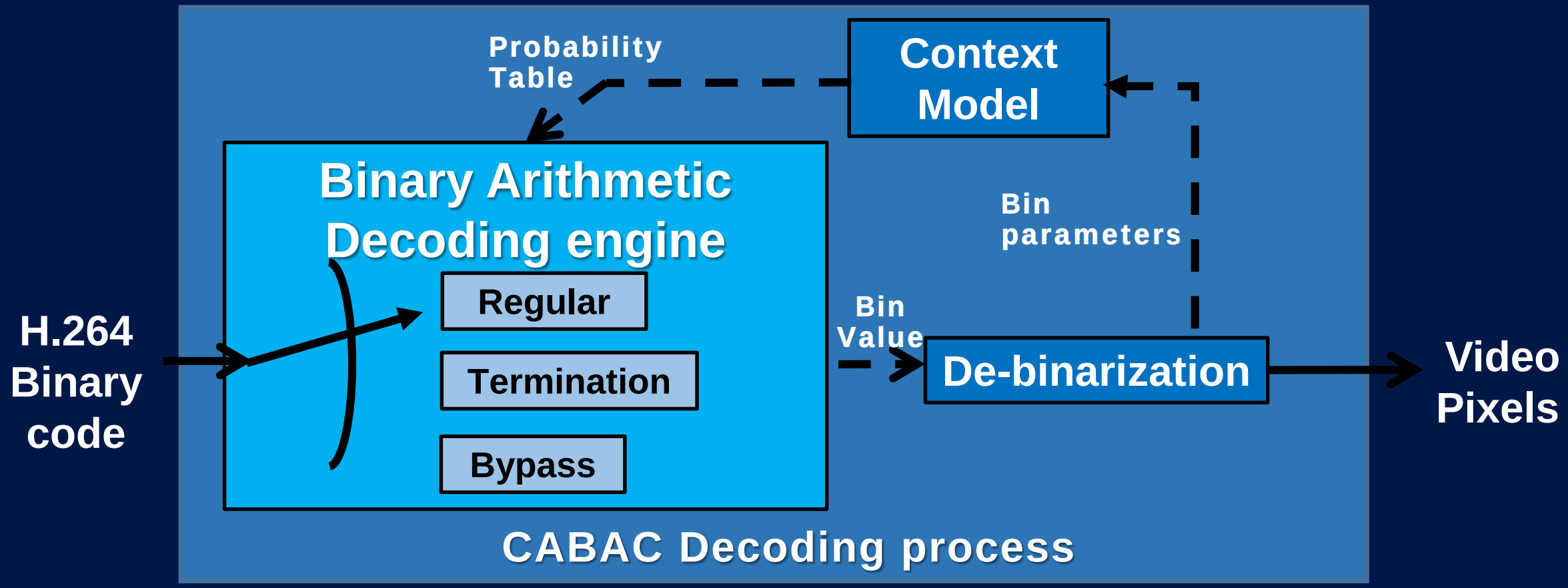
If the *Arithmetic Binary Decoder* code functions are replaced by CABAC Core IP Modules (VHDL implementation) it is possible to decrease the decoding time by at least 10%.

Content

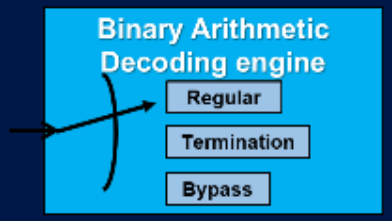
CABAC Block Diagram



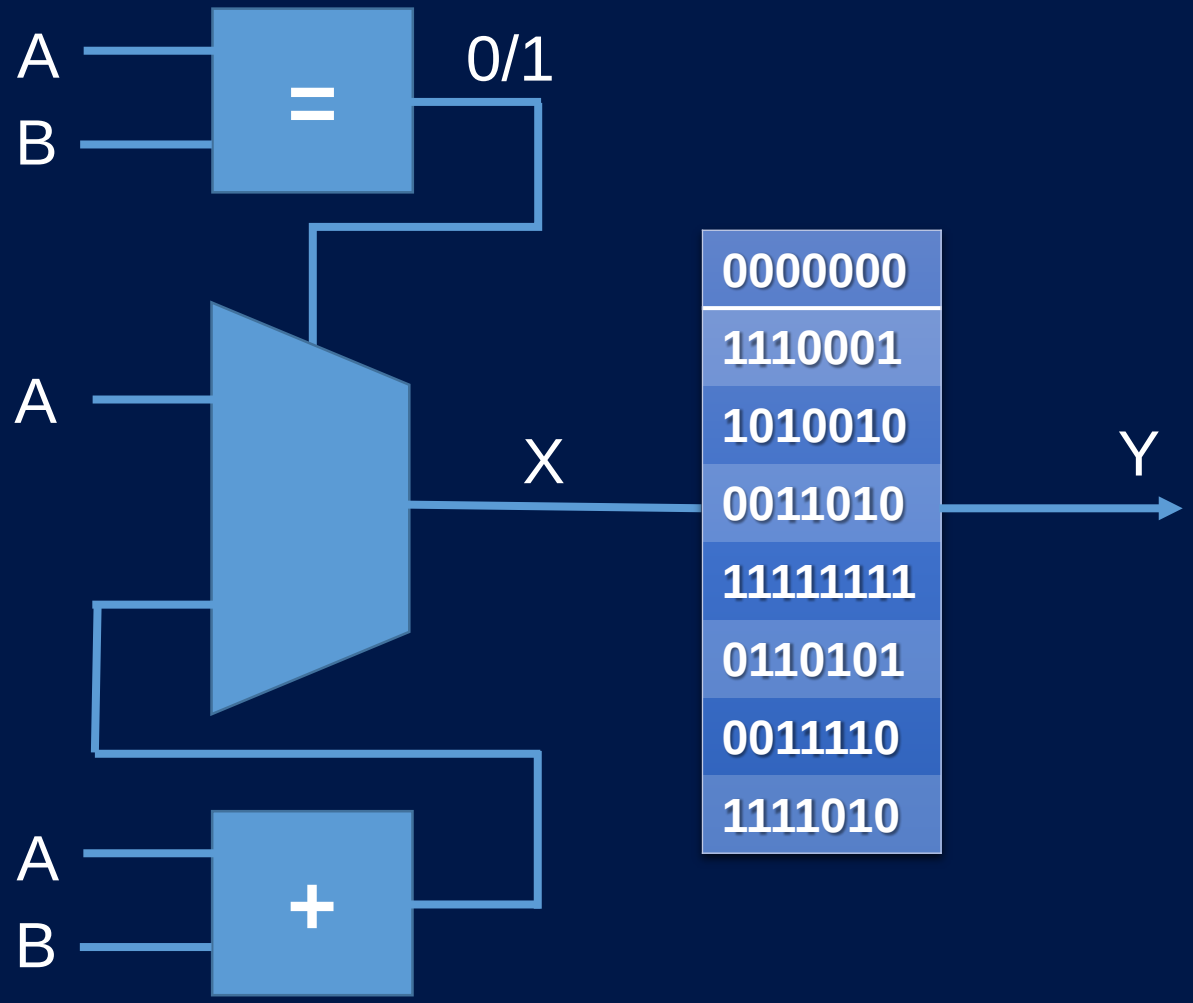
CABAC Block Diagram



Design Block Diagram




```
if (A == B)
{
  X= A;
}
else
{
  X= A+B;
}
Y = FindTable[X];
```



Methodology used to design

Design Insertion in Embedded System

Registers

0	Offset (32 bits)					
1	Range (32 bits)					
2	MPS (1 bits)	Start (2 bit)	WR (1 bit)	Shift (5 bits)	State (6 bits)	Two_Bytes (16 bits)
3	New_Offset (32 bits)					
4	New_Range (32 bits)					
5	New_MPS (1 bits)	End (1 bit)	bin (1 bit)	New_Shift (5 bits)	New_State (6 bits)	Undefined (17 bits)

Content

1 **Scope:** Problematic Situation, Problem, Goal, Hypothesis.

2 **Design:** CABAC Block Diagram, Design Block Diagram, Design Insertion in embedded system on Virtex-5 board.

3 **Results:** Time Diagram of each module, Time analysis of final design.

4 **Conclusions and Recommendations**.

Results of each module

PowerPC Design

- Input
- Output

IP module Design

- Time Diagram

Results of each module (Final Decode)

PowerPC Design

Input

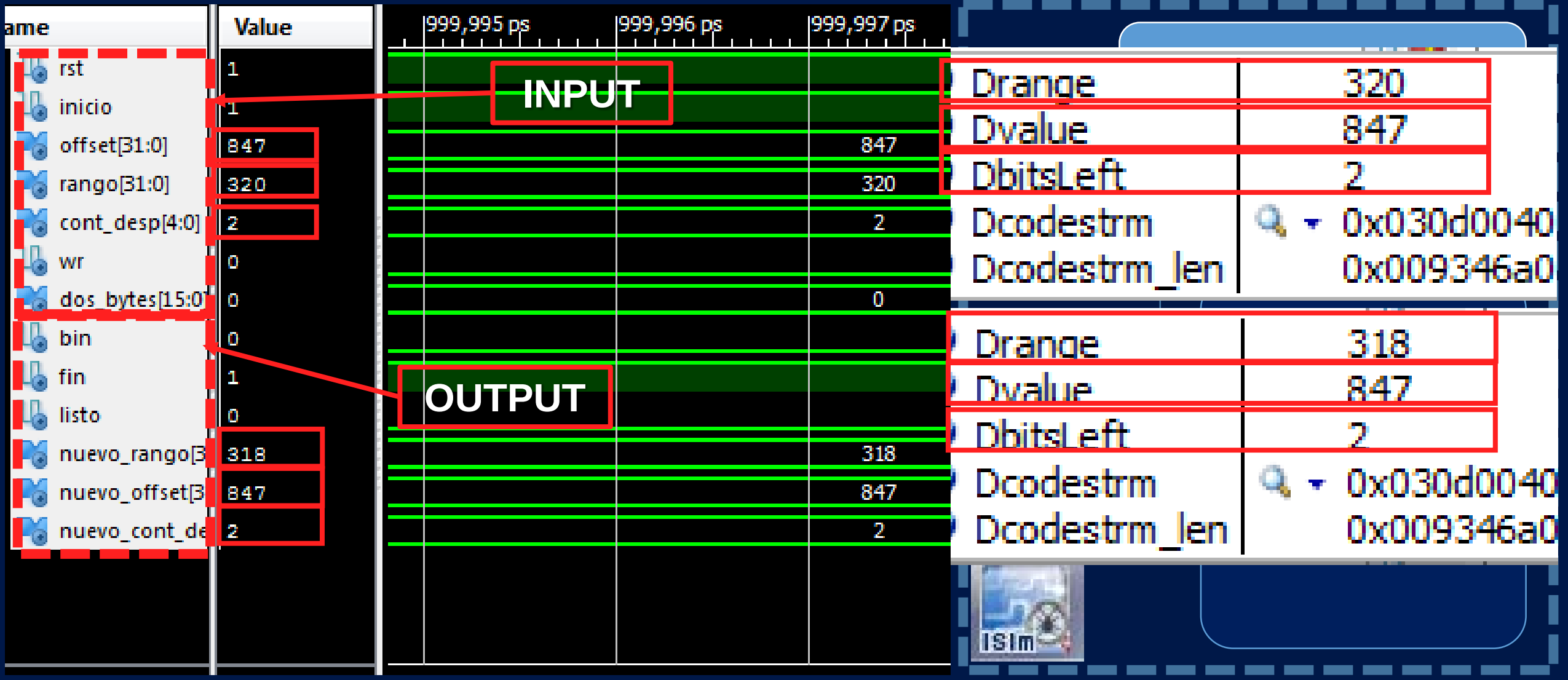
Output

Microsoft® Visual Studio®

	Drange	320
	Dvalue	847
	DbitsLeft	2
⊞	Dcodestrm	0x030d0040
⊞	Dcodestrm_len	0x009346a0

	Drange	318
	Dvalue	847
	DbitsLeft	2
⊞	Dcodestrm	0x030d0040
⊞	Dcodestrm_len	0x009346a0

Results of each module (Final Decode)



Results of each module (Bypass Decode)

PowerPC Design

Input

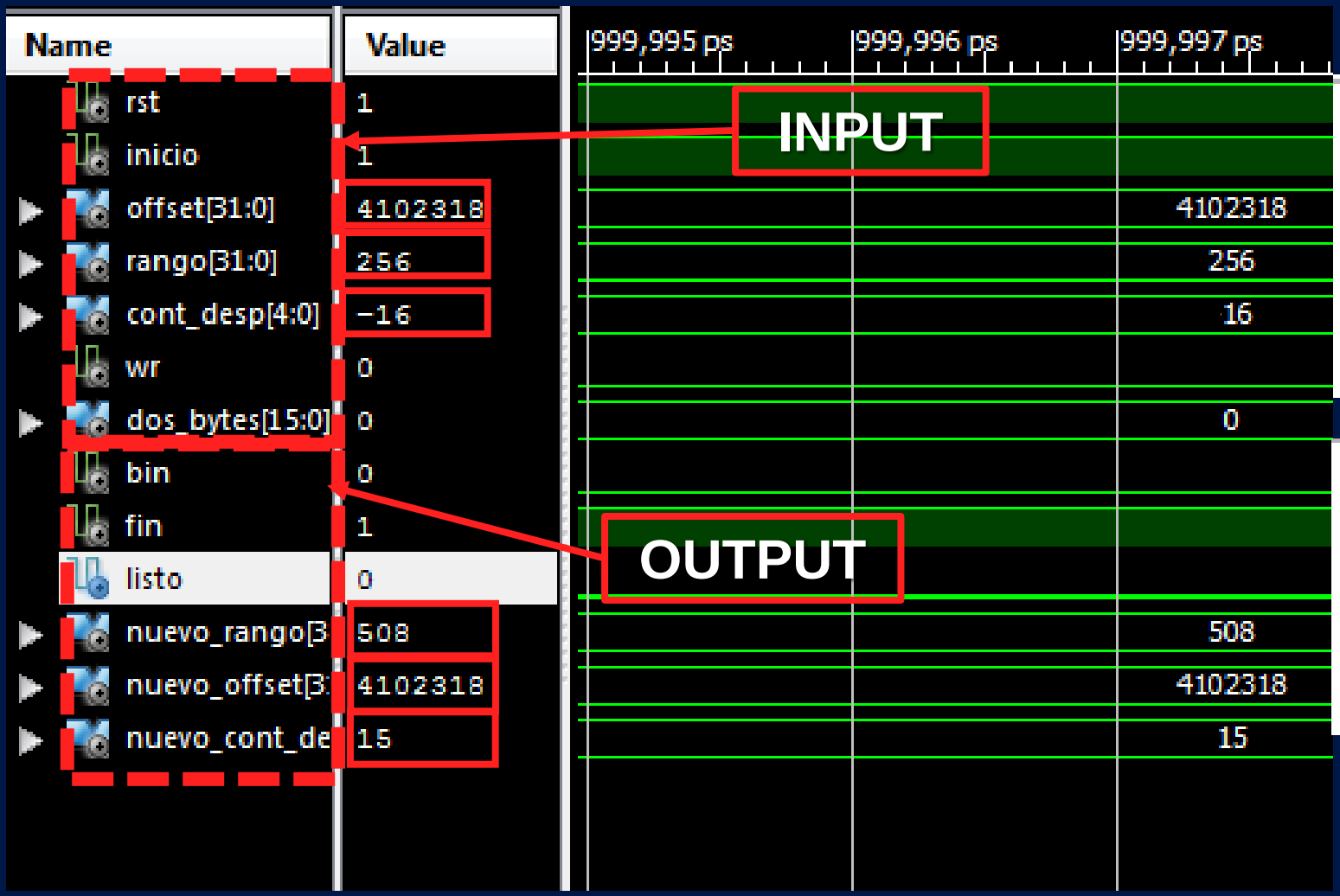
Output

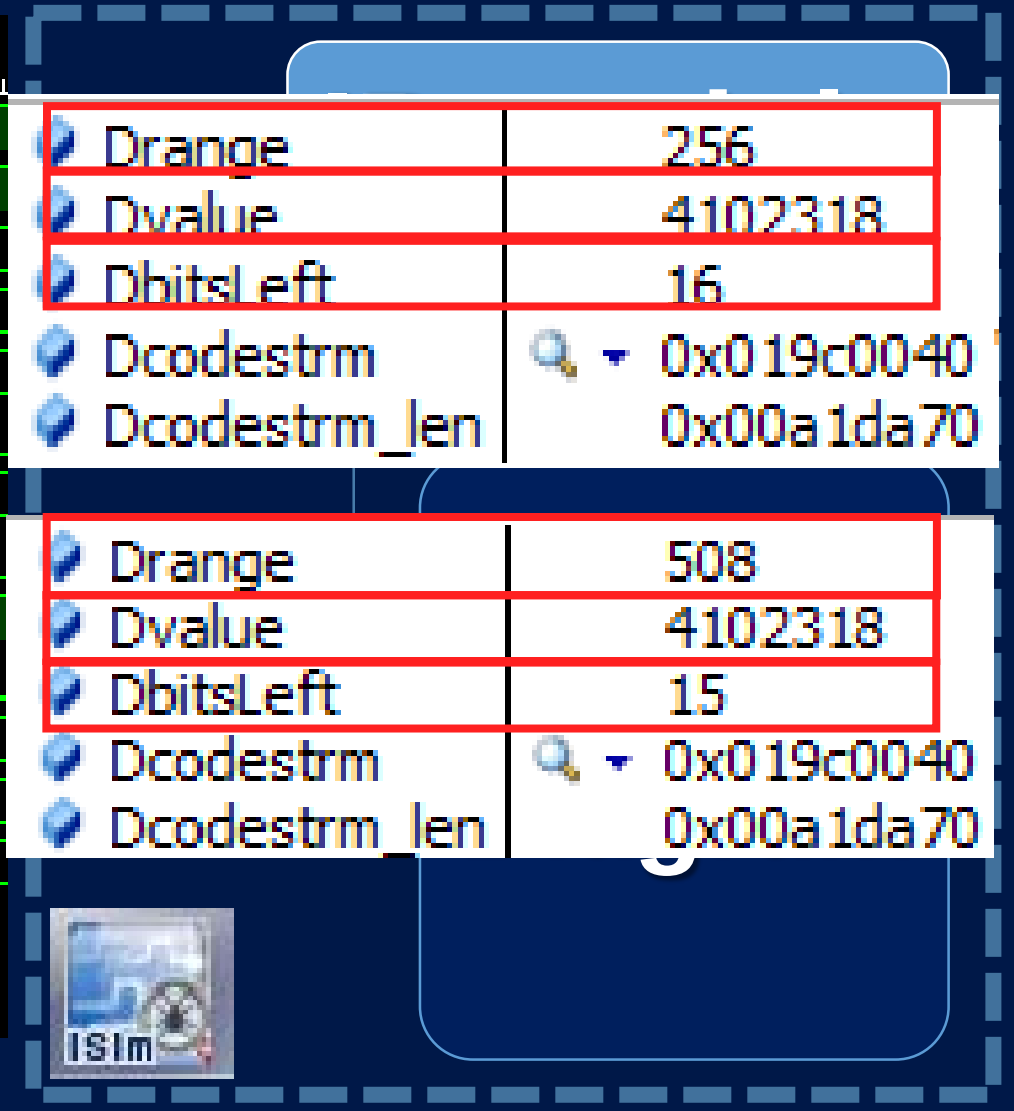
Microsoft® Visual Studio®

Drange	256
Dvalue	4102318
DbitsLeft	16
Dcodestrm	0x019c0040
Dcodestrm_len	0x00a1da70

Drange	508
Dvalue	4102318
DbitsLeft	15
Dcodestrm	0x019c0040
Dcodestrm_len	0x00a1da70

Results of each module (Bypass Decode)





Results of each module (Regular Decode)

PowerPC Design

Input

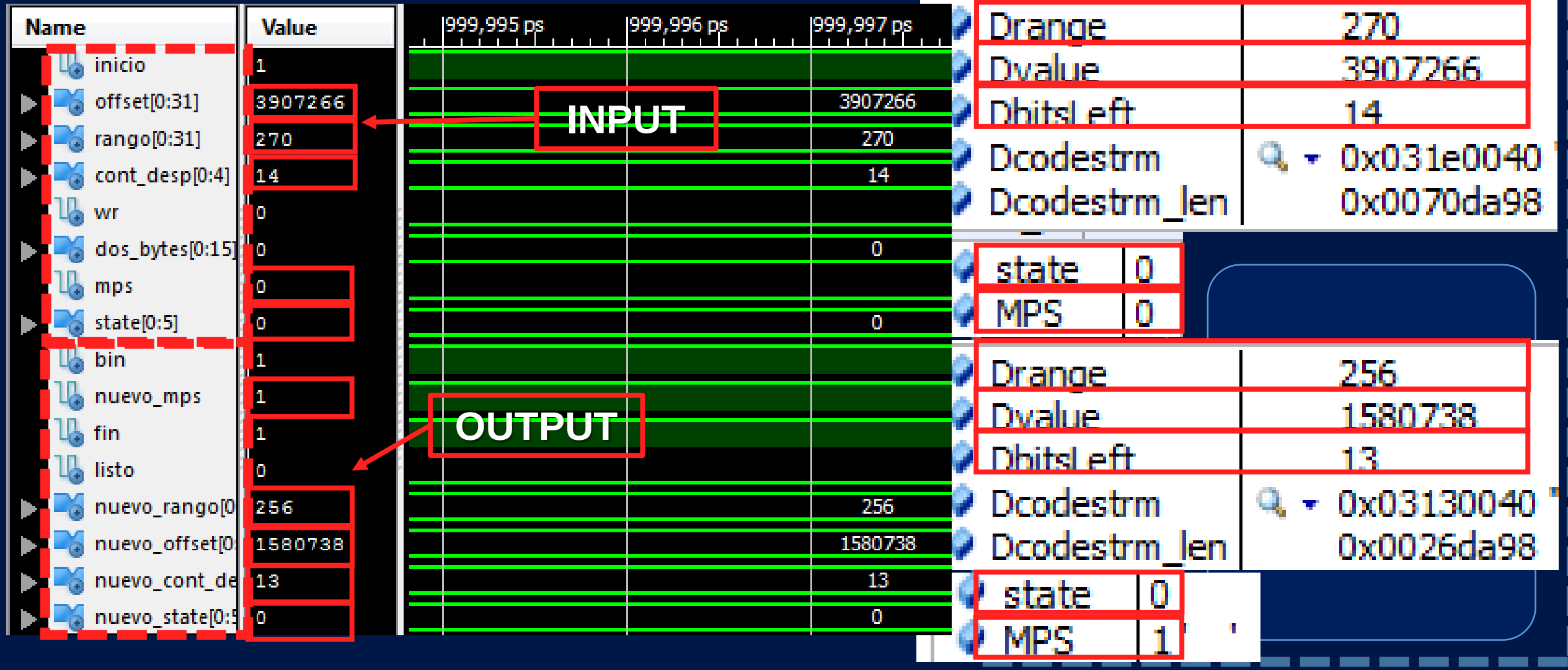
Output

Microsoft® Visual Studio®

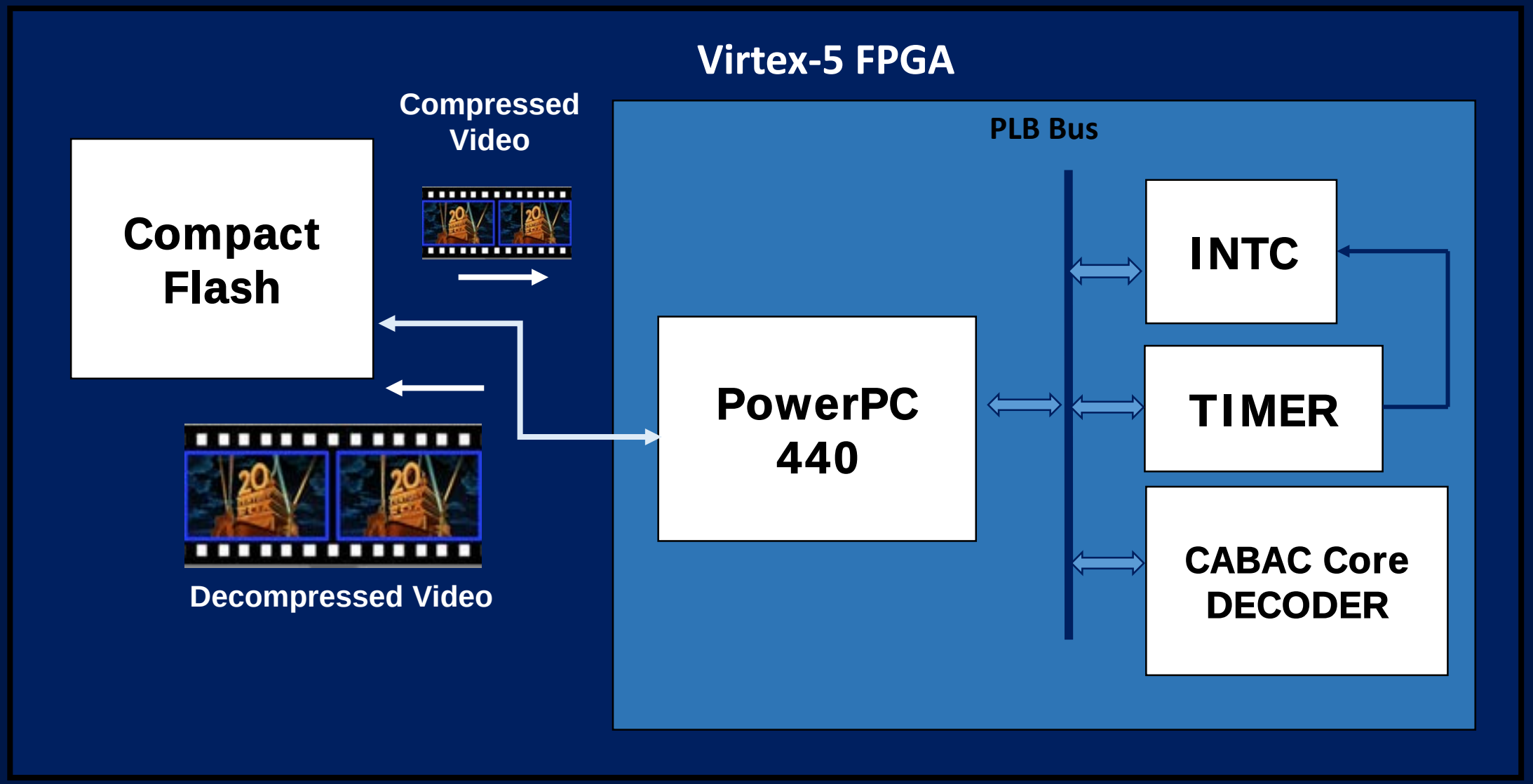
Drange	270
Dvalue	3907266
DbitsLeft	14
Dcodestrm	0x031e0040
Dcodestrm_len	0x0070da98
state	0
MPS	0

Drange	256
Dvalue	1580738
DbitsLeft	13
Dcodestrm	0x03130040
Dcodestrm_len	0x0026da98
state	0
MPS	1

Results of each module (Regular Decode)



Time analysis of final design



Time analysis of final design

H.264 Video	Resolution	Frames	Profile
Video_1	176 x 144	3	Main
Video_2	352 x 240	8	High
Video_3	176 x 144	10	High 4:2:0

$$Time = \frac{value + max\_cont * tmr\_overflow}{bus\_frec}$$

Content

Conclusions

- The CABAC core decoder was designed and embedded into the H.264/AVC decoder system.
- The H.264/AVC decoder temporal performance was evaluated for different experiments and the results showed that CABAC core decoder designed made possible to reduce decoding delay.

Recommendations

- To implement this IP module with a solution with no access to bitstream through read and write software instructions.
- To design all modules with signals 0 to Length-1.
- To design the De-binarization block in next time.

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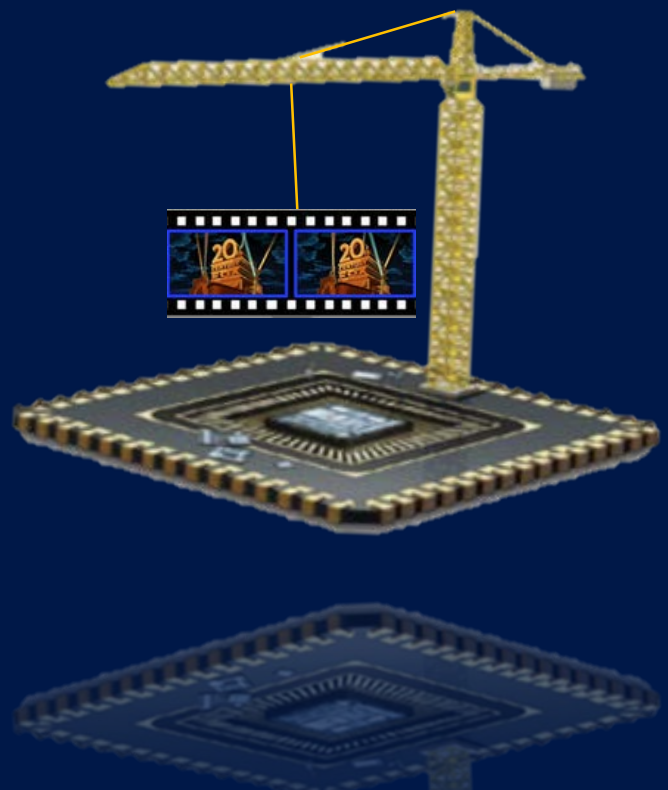

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www.lacetel.cu