

MODELLING an H.264/AVC DECODER USING FPGA.

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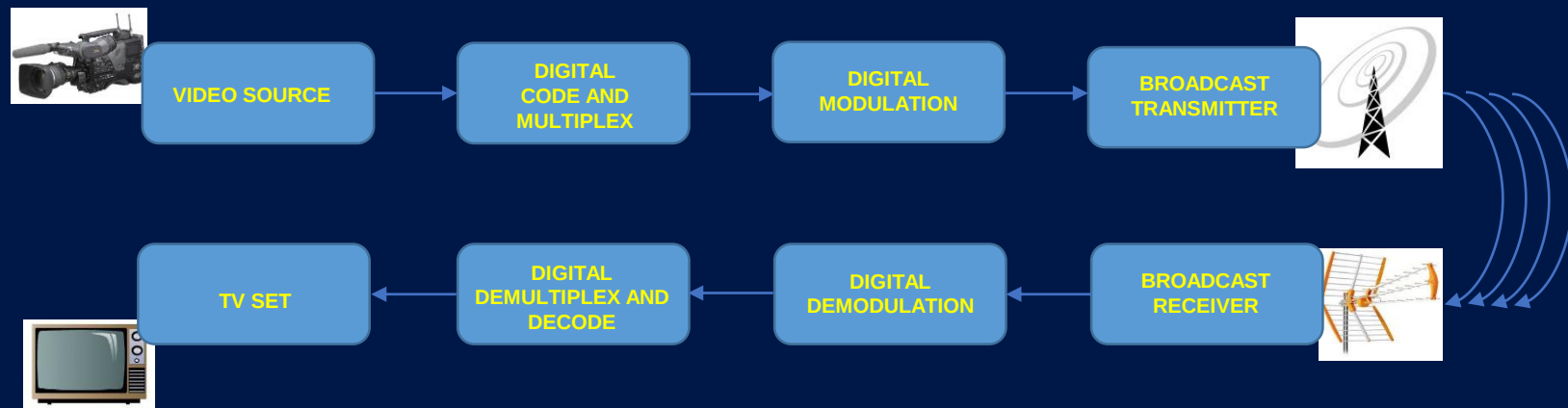
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Introduction (I)

- Cuba is involved in the process of deploying Digital TV (DTV).
- **LACETEL** is leading the technology transference process.
- Solid steps to Technology Independence.

Introduction (II)

Coding and decoding video. DTV chain.



Introduction (III)

ISO/IEC 14496-10 (H.264/AVC o MPEG-4 Part 10).

- Nowadays is the most deployed codec for High Definition TV.

Introduction (IV)

- Mature codec, plenty of scientific documentation, free standard document, free and well organized reference software.
- Existence of H.264/AVC analyzer and player softwares.

PURPOSE

TO DESIGN AND IMPLEMENT AN IDEAL
MODEL OF AN H.264/AVC DECODER USING
FPGA.

Deploying (I)

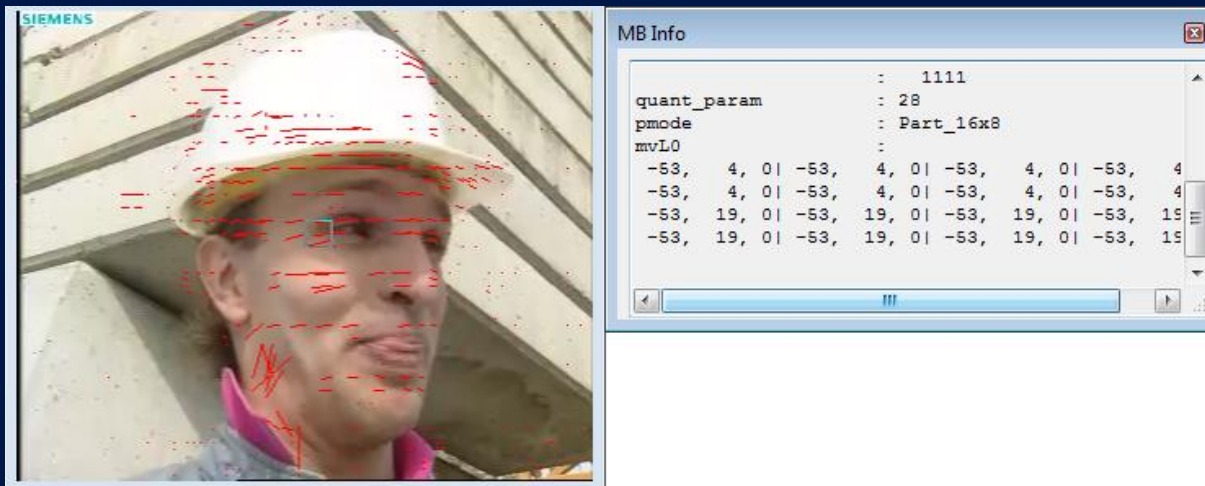
Reference library, version 18.4

- Software described in C language.
- It is the official reference software of the H.264/AVC standard for knowledge and guide.

Deploying (II)

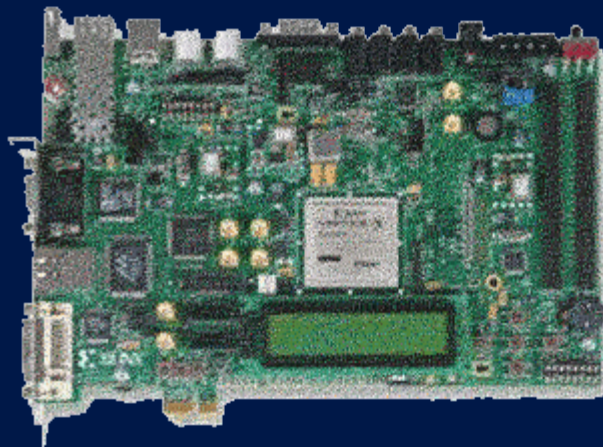
Software compiled in Microsoft Visual Studio.

Tested by Elecard 2.1



Deploying (III)

ML507 development board, from Xilinx. FPGA Virtex 5. PowerPC embedded microprocessor.



Deploying (IV)

- Modification y optimization of the reference software.
- Addtition of read and write features from Compact Flash memory, where are stored the input and output files of the system.

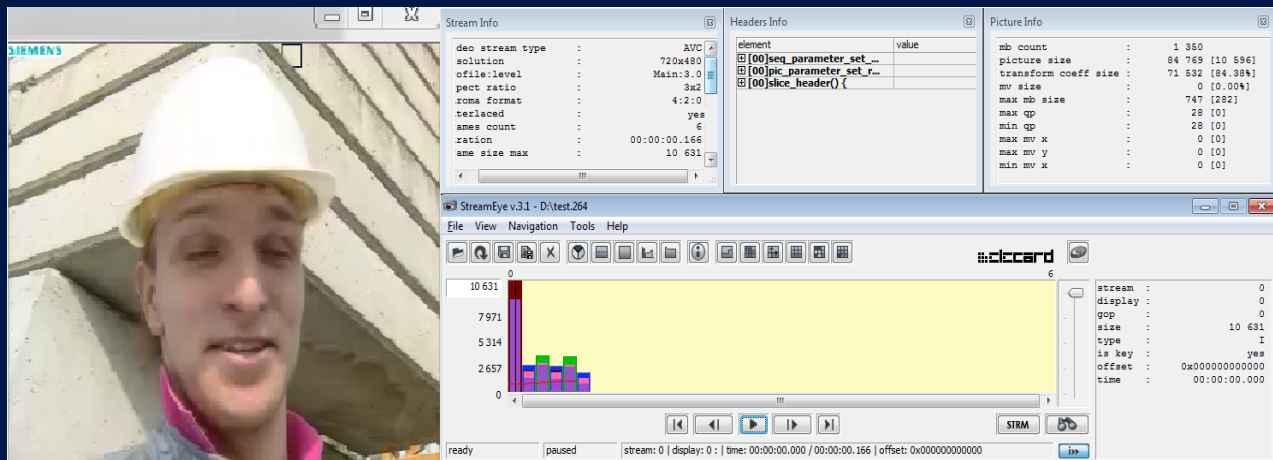
Deploying (V)

- H.264/AVC coded video as input of the decoder model. The process gives as result a decompressed file stored in Compact Flash.



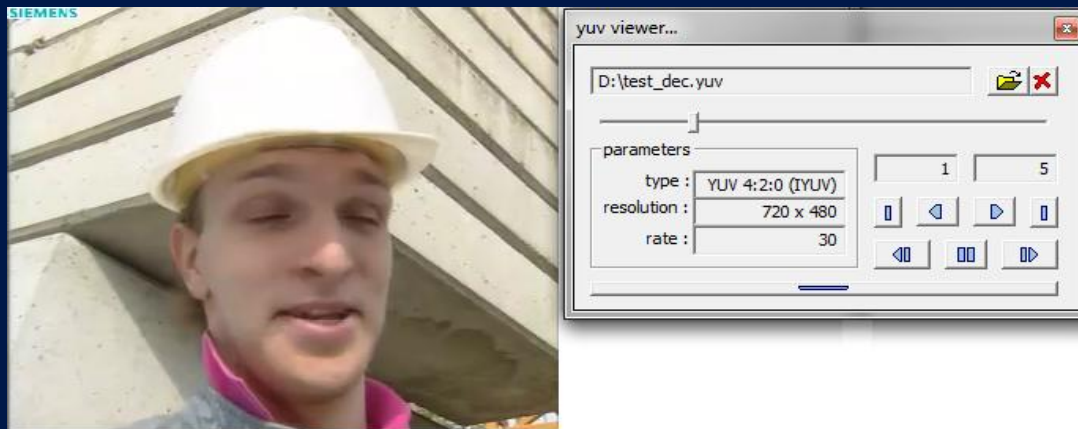
Deploying (VI)

Test of results. Video input consistent with H.264/AVC standard. Elecard 2.1 software.



Deploying (VII)

Test of results. Video output played with YUV software viewer.



Conclusions(I)

- The use of embedded microprocessors into FPGA is a way to build an ideal model of an H.264/AVC decoder.

Conclusions(II)

- Reference software written in C is an important part to H.264/AVC standard documentation.
- Despite the proposed model is not ready to real time application, it does support future optimizations with solid stepflow.

Conclusions(III)

- The proposed model gives the system the guide to achieve real time process and also become the reference for designing and optimization of internal blocks.

Recommendations(I)

- Use hardware/software co-designs to categorize and optimize those blocks who need basic or fast processing. Redefine each one by C language or HDL designs.

Recommendations(II)

- Insert timer features for exact time management. Also modules for display decoded frames, like VGA or DVI interfaces.

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