R&D TELECOM INSTITUTE

DDS IP MODULE LCT3212A

FEATURES:

- 1 GSPS internal clock speed.
- Integrated 12-bit D/A converter.
- RS232 serial control interface.
- 16Kx12 internal ROM memory.
- Either 3.3 V or 5 V power supply.
- 8 frequency profiles with pre-programmable 32-bit register.

APPLICATIONS:

- Digital up/down converters.
- Function Generators.
- Tuners.
- Digital radios and modems.
- Digital Modulators.

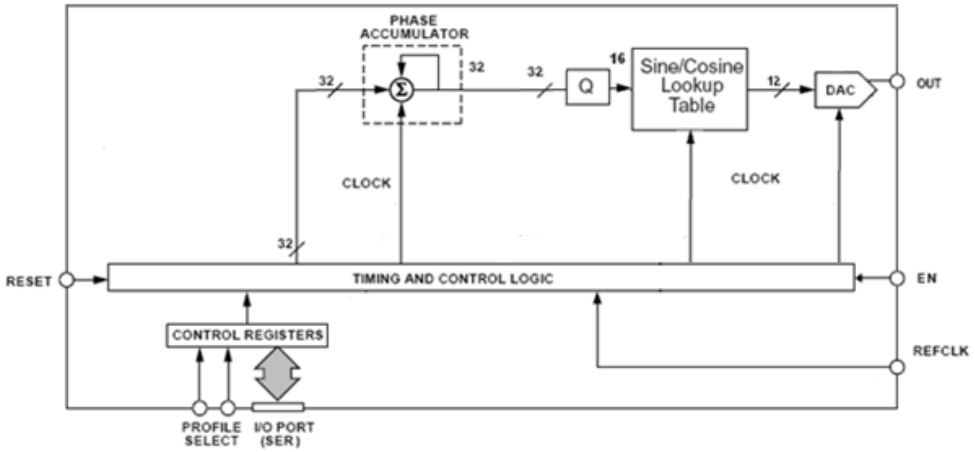
GENERAL DESCRIPTION:

The Direct Digital Synthesizer (DDS) is an important component in many digital communication systems. A common method for digitally generate a sinusoidal waveform, employs a look-up table scheme. The look-up table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the look-up table to obtain the desired output waveform.

The chip includes a 32-bit accumulator, 16Kx12 internal ROM, and a 12 bit DAC to produce one analog output sinusoidal waveform at up to 400 MHz. The device clocks up to 1GHz.

The LCT3212A is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the LCT3212A via RS232 compatible serial interface.

FUNCTIONAL BLOCK DIAGRAM



THEORY OF OPERATION:

The device consists of an integrator (PHASE ACCUMULATOR) that computes a phase slope subsequently mapped by the look-up table to the desired output sinusoidal waveform. The quantizer Q, which is simply a slicer, accepts the high-precision phase angle (32 bits) and generates a lower precision representation of the angle (16 bits). This value is presented to the address port of a look-up table that performs the mapping from phase-space to time. The LCT3212A can directly generate frequencies up to 400 MHz when is driven whit a 1 GHz reference clock signal.

The fidelity of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process. The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively. These resolution limits are equivalent to time base jitter and to amplitude quantization of the signal, and add spectral modulation lines and a white broad-band noise floor to the signal's spectrum. In addition, since the address of the look-up table must be an integer, the fractional part is discarded and the resultant phase jitter is another cause of the spectral artifacts that appear in the spectral domain representation of the output waveform produced by the DDS.

The look-up table stores uniformly spaced samples of a sine wave. Quarter wave symmetry in the basis waveform is exploited to construct a DDS that uses shortened tables. This method results in a more area efficient implementation because the memory requirements are minimized.

The output frequency, of the LCT3212A waveform is a function of the system clock frequency, the number of bits in the phase accumulator and the phase increment value.

That is: $F_O = \frac{(FTW \times \mathrm{REFCLK})}{2^N}$

The frequency resolution is a function of the clock frequency and the number of bits employed in the phase accumulator. The frequency resolution can be determined using the following equation

$$\Delta f = \frac{\mathrm{REFCLK}}{2^N}$$

Where N=32

The frequency resolution of the LCT3212A is 0.233 Hz when the REFCLK is 1 GHz.

The maximum usable frequency in the fundamental range is typically between 40% and 45% of the Nyquist frequency. With a 1 GHz REFCLK, the LCT3212A is capable of producing maximum output frequencies of between 400 MHz and 450 MHz, depending on the reconstruction filter and the application system requirements.

SERIAL PROGRAMMING MODE:

The serial port uses a chip select pin (CS), and 2 serial data pins (DTI and DTO). The DTI pin operates as a serial data input pin, and the DTO pin acts as the serial output. The serial port is an RS232 compatible serial interface.

Serial port communication occurs in two phases. Phase 1 is an instruction cycle consisting of an 8-bit word. The MSB of the command byte flags the ensuing operation as a read or write operation. The 6 LSBs indicate the serial address of the target register as defined in the register map.

D7 (MSB)	D6	D5	D4	D3	D2	D1	DO (LSB)
1: Read 0: Write	X	A5	A4	A3	A2	A1	A0

In the Phase 2 the information is routed to/from the addressed register. The data byte contains the information related with the desired output frequency.

Serial operation requires that all bits associated with a register bank be transferred. The device can be selected by the bus master using a dedicated CS (Chip Select) line.

When CS is taken low, serial communication is enabled, powering-on the DTI and DTO buffers.

REGISTER MAP:

The registers are listed in the table below.

LCT3212A REGISTER MAP

REGISTER NAME	ADDRESS	MSB	B6	B5	B4	B3	B2	B1	LSB
CLEAR	00	Clear FTW7	Clear FTW6	Clear FTW5	Clear FTW4	Clear FTW3	Clear FTW2	Clear FTW1	Clear FTW0
FTW0	01	FTW0(31 DOWNTO 24)							
FTW0	02	FTW0 (23 DOWNTO 16)							
FTW0	03	FTW0 (15 DOWNTO 8)							
FTW0	04	FTW0 (7 DOWNTO 0)							
FTW1	05	FTW1(31 DOWNTO 24)							
FTW1	06	FTW1 (23 DOWNTO 16)							
FTW1	07	FTW1 (15 DOWNTO 8)							
FTW1	08	FTW1 (7 DOWNTO 0)							
FTW2	09	FTW2(31 DOWNTO 24)							
FTW2	10	FTW2 (23 DOWNTO 16)							
FTW2	11	FTW2 (15 DOWNTO 8)							
FTW2	12	FTW2 (7 DOWNTO 0)							
FTW3	13	FTW3(31 DOWNTO 24)							
FTW3	14	FTW3 (23 DOWNTO 16)							
FTW3	15	FTW3 (15 DOWNTO 8)							
FTW3	16	FTW3 (7 DOWNTO 0)							
FTW4	17	FTW4(31 DOWNTO 24)							
FTW4	18	FTW4 (23 DOWNTO 16)							
FTW4	19	FTW4 (15 DOWNTO 8)							
FTW4	20	FTW4 (7 DOWNTO 0)							
FTW5	21	FTW5(31 DOWNTO 24)							
FTW5	22	FTW5 (23 DOWNTO 16)							
FTW5	23	FTW5 (15 DOWNTO 8)							
FTW5	24	FTW5 (7 DOWNTO 0)							
FTW6	25	FTW6(31 DOWNTO 24)							
FTW6	26	FTW6 (23 DOWNTO 16)							
FTW6	27	FTW6 (15 DOWNTO 8)							
FTW6	28	FTW6 (7 DOWNTO 0)							
FTW7	29	FTW7(31 DOWNTO 24)							
FTW7	30	FTW7 (23 DOWNTO 16)							
FTW7	31	FTW7 (15 DOWNTO 8)							
FTW7	32	FTW7 (7 DOWNTO 0)							

REGISTER BIT DESCRIPTIONS:

When **CLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) the Frequency Tuning Word of the corresponding user profile.

FTWX: The output frequency of the DDS is determined by the 32-bit frequency tuning word (FTW) that is loaded into this register. The FTW is supplied by the active profile.

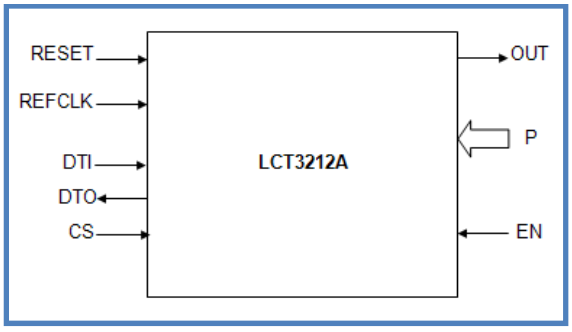
PROFILE SELECTION:

A user profile consists of a specific group of memory registers. In the LCT3212A each profile contains a 32-bit frequency tuning word. Each profile is selectable via three external profile select pins (P1, P2 and P3) as defined in the table below.

P0/P1/P2	USER PROFILE
0/0/0	0
0/0/1	1
0/1/0	2
0/1/1	3
1/0/0	4
1/0/1	5
1/1/0	6
1/1/1	7

The user can set rapid changing of device parameters via these three external pins, which alleviates the speed limitations imposed by the I/O port.

INTERFACE:



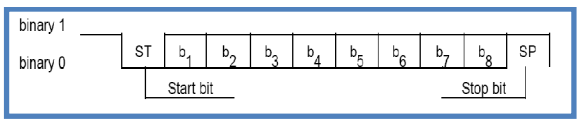
LCT3212A external diagram.

PIN FUNCTION DESCRIPTIONS:

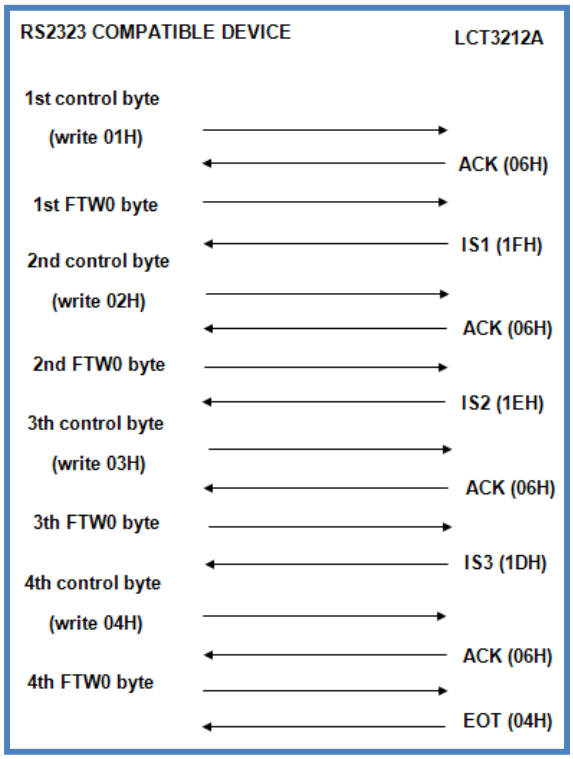
REFCLK	INPUT	Master Clock. Active rising edge.
RESET	INPUT	Synchronous clear. Active high. When RESET is asserted, all registers in the device are cleared.
P	INPUT	Profile select pins (P1, P2 and P3).
CS	INPUT	Chip Select. Each device connected to the serial bus can be selected by the bus master using this line. Active low.
DTI	INPUT	Data In. Line used for serial data reception.
DTO	OUTPUT	Data Out. Line used for serial data transmission.
EN	INPUT	Output Enable.
OUT	OUTPUT	Sine wave output.

ASYNCHRONOUS TRANSMISSION:

To enable fully transparent data transmission an 8-bit character format is used. The characters are transmitted asynchronously with 1 start bit and 1 stop bit. No bit is used for parity checking. The 8-bit code is identified by b8, b7, b6, b5, b4, b3, b2 and b1, where b8 is the most-significant bit (MSB) and b1 is the least-significant bit (LSB).



LCT3212A MESSAGE EXCHANGE EXAMPLE:

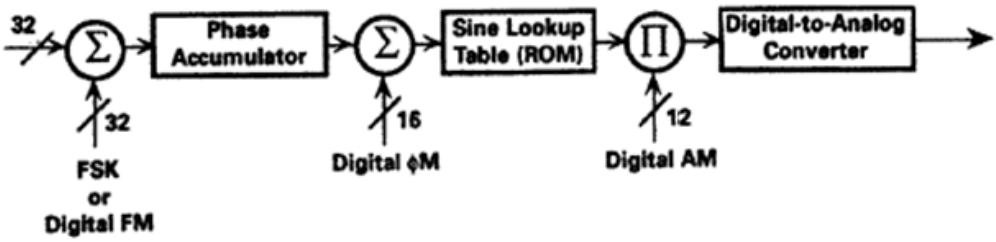


Control Words Definitions:

- **ACK, Acknowledge:** A transmission control character transmitted by a receiver as an affirmative response to the sender.
- **IS1, Information Separator One:** A control character used to separate and qualify data logically; valid reception of the first data byte
- **IS2, Information Separator Two:** A control character used to separate and qualify data logically; valid reception of the second data byte.
- **IS3, Information Separator Three:** A control character used to separate and qualify data logically; valid reception of the third data byte.
- **IS4, Information Separator Four:** A control character used to separate and qualify data logically; valid reception of the fourth data byte.
- **NAK, Negative Acknowledge**: A transmission control character transmitted by a receiver as a negative response to the sender.
- **EOT, End of Transmission**: A transmission control character used to indicate the conclusion of the transmission of one or more data.

All the control characters are defined according to the International Reference Alphabet (IRA) specified in the Recommendation T.50 of the International Telegraph and Telephone Consultative Committee (CCIT).

APPLICATION SUGGESTIONS:



Digital modulation employing a DDS: phase, frequency, and amplitude modulations.

In DDS all parameters are generated digitally and are therefore easy to manipulate. That means that very accurate and fast modulation is easy to implement.

A complete descriptive block diagram is shown in the figure above. The accumulator input is the frequency control port. Since the direct digital synthesizer is switching very fast and is phase-continuous, it is easy to change the frequency and generate frequency modulation (FM).

Phase modulation is easy to implement. Since the output of the accumulator represents the phase of the signal, putting an adder or subtractor between the accumulator and the ROM performs phase modulation, adding or subtracting.

Amplitude modulation is a little more complex to achieve, but, compared to the analog technique, it is very accurate, low cost, and small in size. Since the output of the ROM represents the amplitude of the sine wave, a multiplier between the ROM and the DAC will enable amplitude modulation. Again, since all operations are performed digitally; the accuracy of the AM depends only on the accuracy of the DAC.

Another important modulation that is easy to implement in Direct Digital Synthesizer is pulse modulation. There are two types of pulse modulation in a Direct Digital Synthesizer.

The one resets the whole logic part. This will cause the Direct Digital Synthesizer to be in a known state, denoted as zero phase. When the reset is released, the signal will start to generate its waveform from the same initial phase**.**

A second type of pulse modulation is to reset only the digital data at the input of the DAC. In this case, the whole digital part continues running as usual, but all the input bits to the DAC are 0. In this application, when the reset is canceled, the signal will continue at a phase point where it would be if it had never stopped.

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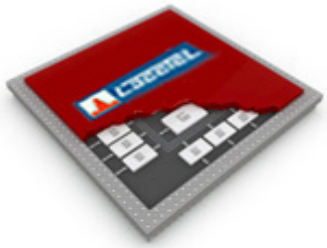

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