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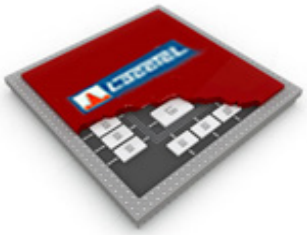
LACETEL® VHDL Soft-Intellectual Property Module



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SpurKiller-DDS IP MODULE

FEATURES:

- 1 GSPS internal clock speed.
- Integrated 12-bit D/A converter.
- RS232 serial control interface.
- 16Kx12 Primary DDS channel ROM memory.
- 10Kx6 Spurkiller DDS channels ROM memory.
- Either 3.3 V or 5 V power supply.
- 8 frequency profiles with pre-programmable 32-bit register.
- 2 SpurKiller channels.

APPLICATIONS:

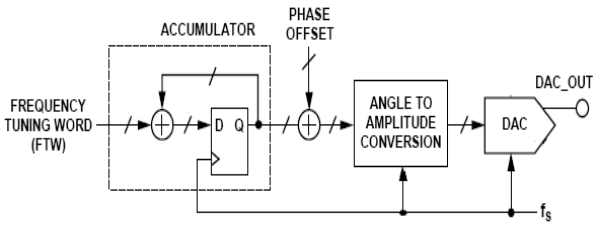
- Digital up/down converters.
- Function Generators.
- Tuners.
- Digital radios and modems.
- Digital Modulators.

GENERAL DESCRIPTION:

The Direct Digital Synthesizer (DDS) is an important component in many digital communication systems. A common method for digitally generate a sinusoidal waveform employing a look-up table scheme. The look-up table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the look-up table to obtain the desired output waveform.

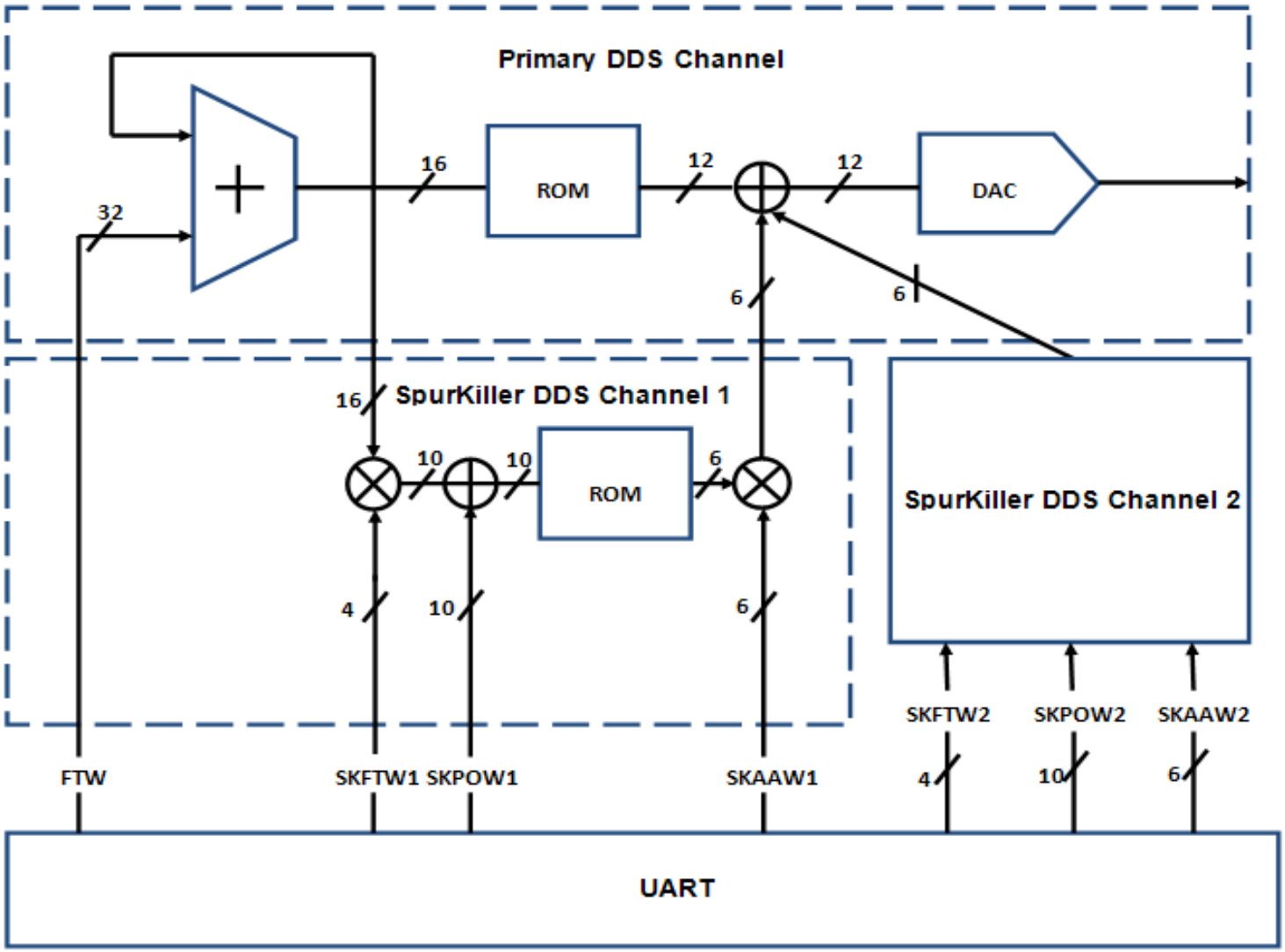
The chip includes a Primary DDS channel, 2 SpurKiller DDS channels and a RS232 serial control interface to produce one analog output sinusoidal waveform at up to 400 MHz employing a digital to analog converter (DAC). The device clocks up to 1GHz.

One DDS channel consists of various digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_s) that serves as the fundamental timing source of the DDS. The accumulator behaves as a modulo-2^{32} counter with a programmable step size (FTW). A block diagram of one DDS channel is shown in the figure below.



The LCT3212C is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the LCT3212C via RS232 compatible serial interface.

LCT3212C FUNCTIONAL BLOCK DIAGRAM



THEORY OF OPERATION:

The Primary DDS channel consists of an integrator (PHASE ACCUMULATOR) that computes a phase slope subsequently mapped by the look-up table to the desired output sinusoidal waveform.

The quantizer Q, which is simply a slicer, accepts the high-precision phase angle (32 bits) and generates a lower precision representation of the angle (16 bits). This value is presented to the address port of a look-up table that performs the mapping from phase-space to time.

The LCT3212C can directly generate frequencies up to 400 MHz when is driven whit a 1 GHz reference clock signal.

The fidelity of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process.

The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively. These resolution limits are equivalent to time base jitter and to amplitude quantization of the signal, and add spectral modulation lines and a white broad-band noise floor to the signal's spectrum.

In addition, since the address of the look-up table must be an integer, the fractional part is discarded and the resultant phase jitter is another cause of the spectral artifacts that appear in the spectral domain representation of the output waveform produced by the DDS.

The look-up table stores uniformly spaced samples of a sine wave. Quarter wave symmetry in the basis waveform is exploited to construct a DDS that uses shortened tables. This method results in a more area efficient implementation because the memory requirements are minimized.

The output frequency of the LCT3212C is a function of the system clock frequency, the number of bits in the phase accumulator and the phase increment value.

That is: $$F_0 = \frac{FTW \times REFCLK}{2^N}$$

The frequency resolution is a function of the clock frequency and the number of bits employed in the phase accumulator. The frequency resolution can be determined using the following equation:

$$\Delta_f = \frac{REFCLK}{2^N}$$

Where N=32.

The frequency resolution of the LCT3212C is 0.233 Hz when the REFCLK is 1 GHz.

The maximum usable frequency in the fundamental range is typically between 40% and 45% of the Nyquist frequency.

With a 1 GHz REFCLK, the LCT3212C can produce maximum output frequencies between 400 MHz and 450 MHz, depending on the reconstruction filter and the application system requirements.

SPURKILLER DDS CHANNELS:

Linearity and quantization errors create undesired harmonics in the DAC/DDS output spectrum, limiting the spurious-free dynamic range (SFDR). Current DDS architecture has been developed to reduce harmonic spurious signals due to the non-ideal characteristics of the DAC, resulting in a significant improvement in SFDR performance.

SpurKiller architecture is based on a technique that is a variation on a method called destructive interference, the method consist on predistort the digital signal as it arrives at the DAC input in such a way that it eliminates the harmonic signal. Summing two sinusoids of the same frequency, but with equal and opposite amplitude, will result in cancellation of both sinusoids. Then a spur can be reduced by combining the original signal with a replica of the spur but offset in phase by 180°. This idea is the foundation of the technique used to reduce harmonic spurious signals.

A basic DDS architecture is comprised of an accumulator, phase to amplitude converter, and a DAC. This structure is ideally suited for the implementation of the destructive interference concept. A cancellation signal can be generated by adding a duplicate DDS path, excluding the DAC.

Two modifications must be made to the primary DDS path. The first is the inclusion of an adder inserted between the primary phase-to-amplitude converter and the DAC in order to facilitate the combining of the cancellation signal with the primary signal. The second is a multiplier that has the primary frequency tuning word as one input and a user-specified frequency scaling value as the other input. This provides the ability to adjust the frequency of the cancellation signal.

In addition to the two changes in the primary DDS path, the "cancellation" DDS also requires two modifications. The first is the insertion of an adder between the accumulator and the input to the phase-to-amplitude converter. This allows the user to apply a phase offset to the cancellation signal relative to the primary signal. The second is a multiplier between the output of the cancellation phase-to-amplitude converter and the input to the adder that now precedes the DAC. This allows the user to scale the amplitude of the cancellation signal.

The cancellation DDS can be designed with less complexity than the primary DDS, because the harmonic spurious signals generated by the DAC are usually very small compared to the primary signal.

One small problem must be taking into account. When the primary and cancellation signals are summed prior to the DAC, an overflow condition will exist. This is because the phase-to-amplitude converter of the primary DDS generates a full-scale sinusoid by design. Any signal added to the full-scale output of the primary phase-to-amplitude converter will necessarily cause an overflow. This is easily prevented by slightly attenuating the output of the primary phase-to-amplitude converter to create enough headroom for the cancellation signal.

The mechanics of performing harmonic spur reduction is shown in the figure below. It essentially consists of two additional DDS cores operating in parallel with the original DDS. This enables the user to reduce two different harmonic spurs from the 2nd to the 15th with 10 bits of phase offset control (0-2π) and 6 bits of amplitude control.

Each SpurKiller Channel has the following User Profile registers:

SpurKiller Frecuency Tuning Word (SKFTW): SpurKiller Channel Frecuency control register.

SpurKiller Phase Offset Word (SKPOW): SpurKiller Channel Phase Offset control register.

SpurKiller Amplitude Adjust Word (SKAAW): SpurKiller Channel Amplitude Adjust control register.

The procedure for tuning the spur reduction is as follows:

1. Determine which offending harmonic spur to reduce. Enter the harmonic number into Bit 0 to Bit 3 of the desire User Profile SKFTW.

2. Turn off the fundamental by setting Bit 6 of Register ENABLE and turn on the SpurKiller channels by setting Bit 0 and/or Bit 3 of Register ENABLE.

3. Adjust the amplitude of the SpurKiller channels so that it matches the amplitude of the offending spur (User Profile SKAAW).

4. Turn the fundamental on by clearing Bit 6 of Register ENABLE.

5. Adjust the phase of the SpurKiller channel so that maximum interference is achieved (User Profile SKPOW).

SERIAL PROGRAMMING MODE:

The serial port uses Clock Source Select pin (SC), and 2 serial data pins (DTI and DTO). The DTI pin operates as a serial data input pin, and the DTO pin acts as the serial output. The serial port is an RS232 compatible serial interface.

Serial port communication occurs in two phases. Phase 1 is an instruction cycle consisting of an 8-bit word. The MSB of the command byte flags the ensuing operation as a read or write operation. The 6 LSBs indicate the serial address of the target register as defined in the register map.

D7 (MSB)	D6	D5	D4	D3	D2	D1	DO (LSB)
1: Read 0: Write	X	A5	A4	A3	A2	A1	A0

In the Phase 2 the information is routed to/from the addressed register. The data byte contains part of the information related with the Frequency Tuning Word of one specific register according to the selected register bank.

Serial operation requires that all bits associated with a register bank be transferred. The number of bytes transferred during Phase 2 depends on the length of the target register bank.

Both phases of a serial port communication require the serial data clock to be operating.

PROFILE SELECTION:

A user profile consists of a specific group of memory registers. In the LCT3212C each profile contains

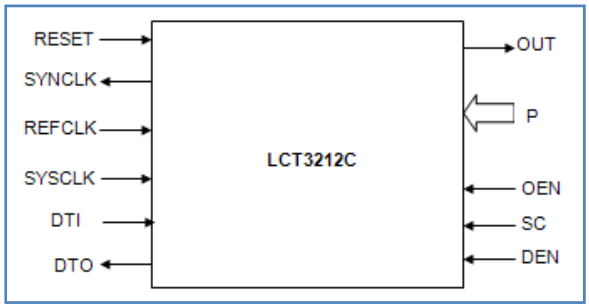
- 32-bit Primary DDS Channel Frequency Tuning Word.
- 8-bit SpurKiller DDS Channel 1 Frecuency Tuning Word.
- 8-bit SpurKiller DDS Channel 2 Frecuency Tuning Word.
- 16-bit SpurKiller DDS Channel 1 Phase Offset Word.
- 16-bit SpurKiller DDS Channel 2 Phase Offset Word.
- 8-bit SpurKiller DDS Channel 1 Amplitude Adjust Word.
- 8-bit SpurKiller DDS Channel 2 Amplitude Adjust Word.

Each profile is selectable via three external profile select pins (P1, P2 and P3) as defined in the table below.

P0/P1/P2	USER PROFILE
0/0/0	0
0/0/1	1
0/1/0	2
0/1/1	3
1/0/0	4
1/0/1	5
1/1/0	6
1/1/1	7

The user can set rapid changing of device parameters via these three external pins, which alleviates the speed limitations imposed by the I/O port.

INTERFACE:



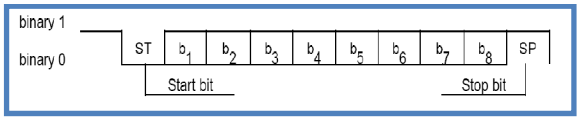
LCT3212C external diagram.

PIN FUNCTION DESCRIPTIONS:

REFCLK	INPUT	Master Clock. Active rising edge.
RESET	INPUT	Asynchronous clear. Active low. When RESET is asserted, all registers in the device are cleared.
P	INPUT	Profile select pins (P1, P2 and P3).
SC	INPUT	Clock Source Select. Signal used for select between an external or internal RS232 interface clock source. High level. External clock source. Low level. Internal clock source.
SYSCLK	INPUT	External RS232 interface clock source.
SYNCLK	OUTPUT	Clock Output Pin. Serves as a synchronization signal for the RS232 interface when is connected to the SYSCLK pin.
DTI	INPUT	Data In. Line used for serial data reception.
DTO	OUTPUT	Data Out. Line used for serial data transmission.
OEN	INPUT	Output Enable. Active high.
DEN	INPUT	High level. Phase Dithered DDS Enable. Low level. Simple DDS Enable.
OUT	OUTPUT	Sinusoidal waveform output.

ASYNCHRONOUS TRANSMISSION:

To enable fully transparent data transmission an 8-bit character format is used. The characters are transmitted asynchronously with 1 start bit and 1 stop bit. No bit is used for parity checking. The 8-bit code is identified by b8, b7, b6, b5, b4, b3, b2 and b1, where b8 is the most-significant bit (MSB) and b1 is the least-significant bit (LSB).



SYSTEM CLOCKING:

Timing for the LCT3212C is provided via the user-supplied REFCLK input. The REFCLK input is buffered and is the source for the internally generated SYNCLK signal. The frequency of the signal SYNCLK is a function of the clock frequency REFCLK and can be determined using the following equation:

$$\mathbf{SYNCLK} = \frac{\mathbf{REFCLK}}{\mathbf{6510}}$$

The user can supply the reference signal for the RS232 communication interface both internally or externally by means of the SC pin.

The serial communication reference signal can be provide internally setting low the SC pin in the following cases:

REFCLK FRECUENCY	SYNCLK FRECUENCY	DATA RATE BITS PER SECOND
1GHz	153600 Hz	9600 bps
500MHz	76800 Hz	4800 bps
250MHz	38400 Hz	2400 bps
125MHz	19200 Hz	1200 bps

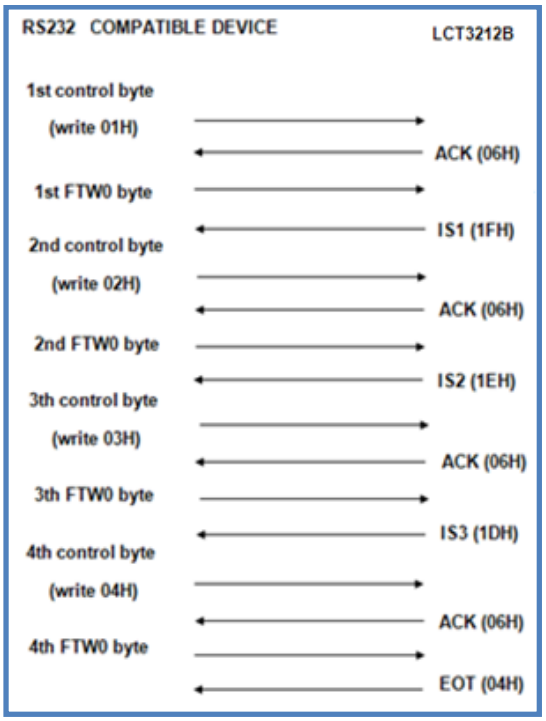
Thus, when the reference signal is supply internally it's mandatory that the REFCLK frequency be one of the values related in the above table.

Besides, the reference signal can be externally provided via the SYSCLK pin as follows:

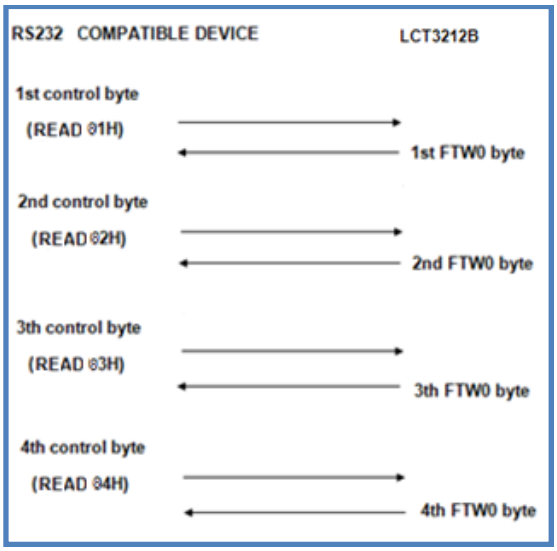
SYSCLK FRECUENCY	DATA RATE BITS PER SECOND
153600 Hz	9600 bps
76800 Hz	4800 bps
38400 Hz	2400 bps
19200 Hz	1200 bps

The SYNCLK pin is used to give an external synchronization clock, and it's the same internal SYNCLK signal based on the REFCLK input.

LCT3212C WRITE MESSAGE EXCHANGE EXAMPLE:



LCT3212C READ MESSAGE EXCHANGE EXAMPLE:



Control Words Definitions:

- **ACK, Acknowledge:** A transmission control character transmitted by a receiver as an affirmative response to the sender.
- **IS1, Information Separator One:** A control character used to separate and qualify data logically; valid reception of the first data byte
- **IS2, Information Separator Two:** A control character used to separate and qualify data logically; valid reception of the second data byte.
- **IS3, Information Separator Three:** A control character used to separate and qualify data logically; valid reception of the third data byte.
- **IS4, Information Separator Four:** A control character used to separate and qualify data logically; valid reception of the fourth data byte.
- **NAK, Negative Acknowledge**: A transmission control character transmitted by a receiver as a negative response to the sender.
- **EOT, End of Transmission**: A transmission control character used to indicate the conclusion of the transmission of one or more data.

All the control characters are defined according to the International Reference Alphabet (IRA) specified in the Recommendation T.50 of the International Telegraph and Telephone Consultative Committee (CCIT).

REGISTER MAP:

LCT3212C REGISTER MAP TABLE 1									
REGISTER NAME	**ADDRESS**	**MSB**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**LSB**
CLEAR	00	Clear FTW7	Clear FTW6	Clear FTW5	Clear FTW4	Clear FTW3	Clear FTW2	Clear FTW1	Clear FTW0
FTW0	01	FTW0(31 DOWNTO 24)							
FTW0	02	FTW0 (23 DOWNTO 16)							
FTW0	03	FTW0 (15 DOWNTO 8)							
FTW0	04	FTW0 (7 DOWNTO 0)							
FTW1	05	FTW1(31 DOWNTO 24)							
FTW1	06	FTW1 (23 DOWNTO 16)							
FTW1	07	FTW1 (15 DOWNTO 8)							
FTW1	08	FTW1 (7 DOWNTO 0)							
FTW2	09	FTW2(31 DOWNTO 24)							
FTW2	10	FTW2 (23 DOWNTO 16)							
FTW2	11	FTW2 (15 DOWNTO 8)							
FTW2	12	FTW2 (7 DOWNTO 0)							
FTW3	13	FTW3(31 DOWNTO 24)							
FTW3	14	FTW3 (23 DOWNTO 16)							
FTW3	15	FTW3 (15 DOWNTO 8)							
FTW3	16	FTW3 (7 DOWNTO 0)							
FTW4	17	FTW4(31 DOWNTO 24)							
FTW4	18	FTW4 (23 DOWNTO 16)							
FTW4	19	FTW4 (15 DOWNTO 8)							
FTW4	20	FTW4 (7 DOWNTO 0)							
FTW5	21	FTW5(31 DOWNTO 24)							
FTW5	22	FTW5 (23 DOWNTO 16)							
FTW5	23	FTW5 (15 DOWNTO 8)							
FTW5	24	FTW5 (7 DOWNTO 0)							
FTW6	25	FTW6(31 DOWNTO 24)							
FTW6	26	FTW6 (23 DOWNTO 16)							
FTW6	27	FTW6 (15 DOWNTO 8)							
FTW6	28	FTW6 (7 DOWNTO 0)							
FTW7	29	FTW7(31 DOWNTO 24)							
FTW7	30	FTW7 (23 DOWNTO 16)							
FTW7	31	FTW7 (15 DOWNTO 8)							
FTW7	32	FTW7 (7 DOWNTO 0)							

LCT3212C REGISTER MAP
TABLE 2

REGISTER NAME	ADDRESS	MSB	B6	B5	B4	B3	B2	B1	LSB
SK1FTW0	33	Reserved	Reserved	Reserved	Reserved	SK1FTW0(3 DOWNTO 0)			
SK1POW0	34	SK1POW0(7 DOWNTO 0)							
SK1POW0	35	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW0(9 DOWNTO 8)	
SK1AAW0	36	Reserved	Reserved	SK1AAW0 (5 DOWNTO 0)					
SK1FTW1	37	Reserved	Reserved	Reserved	Reserved	SK1FTW1(3 DOWNTO 0)			
SK1POW1	38	SK1POW1(7 DOWNTO 0)							
SK1POW1	39	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW1(9 DOWNTO 8)	
SK1AAW1	40	Reserved	Reserved	SK1AAW1 (5 DOWNTO 0)					
SK1FTW2	41	Reserved	Reserved	Reserved	Reserved	SK1FTW2(3 DOWNTO 0)			
SK1POW2	42	SK1POW2(7 DOWNTO 0)							
SK1POW2	43	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW2(9 DOWNTO 8)	
SK1AAW2	44	Reserved	Reserved	SK1AAW2 (5 DOWNTO 0)					
SK1FTW3	45	Reserved	Reserved	Reserved	Reserved	SK1FTW3(3 DOWNTO 0)			
SK1POW3	46	SK1POW3(7 DOWNTO 0)							
SK1POW3	47	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW3(9 DOWNTO 8)	
SK1AAW3	48	Reserved	Reserved	SK1AAW3 (5 DOWNTO 0)					
SK1FTW4	49	Reserved	Reserved	Reserved	Reserved	SK1FTW4(3 DOWNTO 0)			
SK1POW4	50	SK1POW4(7 DOWNTO 0)							
SK1POW4	51	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW4(9 DOWNTO 8)	
SK1AAW4	52	Reserved	Reserved	SK1AAW4 (5 DOWNTO 0)					
SK1FTW5	53	Reserved	Reserved	Reserved	Reserved	SK1FTW5(3 DOWNTO 0)			
SK1POW5	54	SK1POW5(7 DOWNTO 0)							
SK1POW5	55	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW5(9 DOWNTO 8)	
SK1AAW5	56	Reserved	Reserved	SK1AAW5 (5 DOWNTO 0)					
SK1FTW6	57	Reserved	Reserved	Reserved	SK1FTW6(3 DOWNTO 0)				
SK1POW6	58	SK1POW6(7 DOWNTO 0)							
SK1POW6	59	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW6(9 DOWNTO 8)	
SK1AAW6	60	Reserved	Reserved	SK1AAW6 (5 DOWNTO 0)					
SK1FTW7	61	Reserved	Reserved	Reserved	Reserved	SK1FTW7(3 DOWNTO 0)			
SK1POW7	62	SK1POW7(7 DOWNTO 0)							
SK1POW7	63	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK1POW7(9 DOWNTO 8)	
SK1AAW7	64	Reserved	Reserved	SK1AAW7 (5 DOWNTO 0)					
SK1FTWCLEAR	65	Clear SK1FTW7	Clear SK1FTW6	Clear SK1FTW5	Clear SK1FTW4	Clear SK1FTW3	Clear SK1FTW2	Clear SK1FTW1	Clear SK1FTW0
SK1POWCLEAR	66	Clear SK1POW7	Clear SK1POW6	Clear SK1POW5	Clear SK1POW4	Clear SK1POW3	Clear SK1POW2	Clear SK1POW1	Clear SK1POW0
SK1AAWCLEAR	67	Clear SK1AAW7	Clear SK1AAW6	Clear SK1AAW5	Clear SK1AAW4	Clear SK1AAW3	Clear SK1AAW2	Clear SK1AAW1	Clear SK1AAW0

LCT3212C REGISTER MAP
TABLE 3

REGISTER NAME	ADDRESS	MSB	B6	B5	B4	B3	B2	B1	LSB
SK2FTW0	68	Reserved	Reserved	Reserved	Reserved	SK2FTW0(3 DOWNTO 0)			
SK2POW0	69	SK2POW0(7 DOWNTO 0)							
SK2POW0	70	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW0(9 DOWNTO 8)	
SK2AAW0	71	Reserved	Reserved	SK2AAW0 (5 DOWNTO 0)					
SK2FTW1	72	Reserved	Reserved	Reserved	Reserved	SK2FTW1(3 DOWNTO 0)			
SK2POW1	73	SK2POW1(7 DOWNTO 0)							
SK2POW1	74	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW1(9 DOWNTO 8)	
SK2AAW1	75	Reserved	Reserved	SK2AAW1 (5 DOWNTO 0)					
SK2FTW2	76	Reserved	Reserved	Reserved	Reserved	SK2FTW2(3 DOWNTO 0)			
SK2POW2	77	SK2POW2(7 DOWNTO 0)							
SK2POW2	78	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW2(9 DOWNTO 8)	
SK2AAW2	79	Reserved	Reserved	SK2AAW2 (5 DOWNTO 0)					
SK2FTW3	80	Reserved	Reserved	Reserved	Reserved	SK2FTW3(3 DOWNTO 0)			
SK2POW3	81	SK2POW3(7 DOWNTO 0)							
SK2POW3	82	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW3(9 DOWNTO 8)	
SK2AAW3	84	Reserved	Reserved	SK2AAW3 (5 DOWNTO 0)					
SK2FTW4	85	Reserved	Reserved	Reserved	Reserved	SK2FTW4(3 DOWNTO 0)			
SK2POW4	86	SK2POW4(7 DOWNTO 0)							
SK2POW4	87	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW4(9 DOWNTO 8)	
SK2AAW4	88	Reserved	Reserved	SK2AAW4 (5 DOWNTO 0)					
SK2FTW5	89	Reserved	Reserved	Reserved	Reserved	SK2FTW5(3 DOWNTO 0)			
SK2POW5	90	SK2POW5(7 DOWNTO 0)							
SK2POW5	91	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW5(9 DOWNTO 8)	
SK2AAW5	92	Reserved	Reserved	SK2AAW5 (5 DOWNTO 0)					
SK2FTW6	93	Reserved	Reserved	Reserved	SK2FTW6(3 DOWNTO 0)				
SK2POW6	94	SK2POW6(7 DOWNTO 0)							
SK2POW6	95	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW6(9 DOWNTO 8)	
SK2AAW6	96	Reserved	Reserved	SK2AAW6 (5 DOWNTO 0)					
SK2FTW7	97	Reserved	Reserved	Reserved	Reserved	SK2FTW7(3 DOWNTO 0)			
SK2POW7	98	SK2POW7(7 DOWNTO 0)							
SK2POW7	99	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SK2POW7(9 DOWNTO 8)	
SK2AAW7	100	Reserved	Reserved	SK2AAW7 (5 DOWNTO 0)					
SK2FTWCLEAR	101	Clear SK2FTW7	Clear SK2FTW6	Clear SK2FTW5	Clear SK2FTW4	Clear SK2FTW3	Clear SK2FTW2	Clear SK2FTW1	Clear SK2FTW0
SK2POWCLEAR	102	Clear SK2POW7	Clear SK2POW6	Clear SK2POW5	Clear SK2POW4	Clear SK2POW3	Clear SK2POW2	Clear SK2POW1	Clear SK2POW0
SK2AAWCLEAR	103	Clear SK2AAW7	Clear SK2AAW6	Clear SK2AAW5	Clear SK2AAW4	Clear SK2AAW3	Clear SK2AAW2	Clear SK2AAW1	Clear SK2AAW0
ENABLE	104	SK CH1 EN	SK CH1 POEN	SK CH1 AAEN	SK CH2 EN	SK CH2 POEN	SK CH2 AAEN	PR CH EN	Reserved

REGISTERS DESCRIPTION:

FTWX: The output frequency of the Primary DDS Channel is determined by the 32-bit Frequency Tuning Word (FTW) that is loaded into this register. The FTW is supplied by the active profile.

When **CLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) the Frequency Tuning Word of the corresponding User Profile.

When **SK1FTWCLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) SpurKiller DDS Channel 1 Frequency Tuning Word of the corresponding User Profile.

When **SK1POWCLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) the SpurKiller DDS Channel 1 Phase Offset Word of the corresponding User Profile.

When **SK1AAWCLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) the SpurKiller DDS Channel 1 Amplitude Adjust Word of the corresponding User Profile.

When **SK2FTWCLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) SpurKiller DDS Channel 2 Frequency Tuning Word of the corresponding User Profile.

When **SK2POWCLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) the SpurKiller DDS Channel 2 Phase Offset Word of the corresponding User Profile.

When **SK2AAWCLEAR** (B_X) = 1: Automatically synchronously clears (loads zeros into) the SpurKiller DDS Channel 2 Amplitude Adjust Word of the corresponding User Profile.

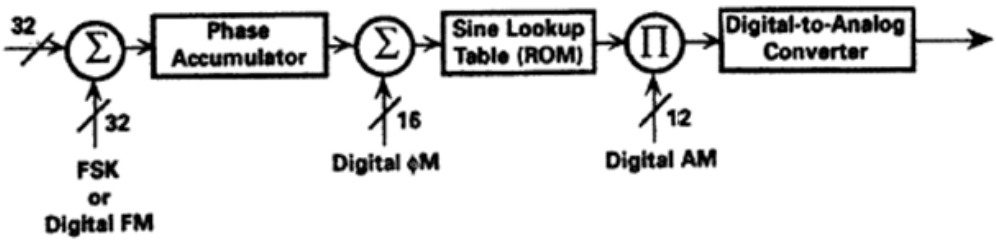
SK(X)FTW(X): The output frequency of the SpurKiller DDS Channel is determined by the binary word loaded into this register. The **SKFTW** is supplied by the active profile. Allows user to choose which harmonic to eliminate.

SK(X)POW(X): Allows user to vary the phase of the SpurKiller DDS Channel output. The **SKPOW** is supplied by the active profile.

SK(X)AAW(X): Linear multiplier for SpurKiller DDS Channel output. Register employed to adjust the amplitude of the SpurKiller Channel so that it matches the amplitude of the offending spur. The **SKAAW** is supplied by the active profile.

ENABLE: SK CH(X) EN: SpurKiller DDS Channel (X) enable**,** active high. **SK CH(X) POEN:** SpurKiller DDS Channel (X) Phase Offset enable, active high. **SK CH(X) AAEN:** SpurKiller DDS Channel (X) Amplitude Adjust enable, active high. **PR CH EN** Primary DDS Channel enable, active low.

APPLICATION SUGGESTIONS:



Digital modulation employing a DDS: phase, frequency, and amplitude modulations.

In DDS all parameters are generated digitally and are therefore easy to manipulate. That means that very accurate and fast modulation is easy to implement.

A complete descriptive block diagram is shown in the figure above. The accumulator input is the frequency control port. Since the direct digital synthesizer is switching very fast and is phase-continuous, it is easy to change the frequency and generate frequency modulation (FM).

Phase modulation is easy to implement. Since the output of the accumulator represents the phase of the signal, putting an adder or subtractor between the accumulator and the ROM performs phase modulation, adding or subtracting.

Amplitude modulation is a little more complex to achieve, but, compared to the analog technique, it is very accurate, low cost, and small in size. Since the output of the ROM represents the amplitude of the sine wave, a multiplier enable amplitude modulation. Again, since all operations are performed digitally; the accuracy of the AM depends only on the accuracy of the DAC.

Another important modulation that is easy to implement in Direct Digital Synthesizer is pulse modulation. There are two types of pulse modulation in a Direct Digital Synthesizer.

The one resets the whole logic part. This will cause the Direct Digital Synthesizer to be in a known state, denoted as zero phase. When the reset is released, the signal will start to generate its waveform from the same initial phase.

A second type of pulse modulation is to reset only the digital data at the input of the DAC. In this case, the whole digital part continues running as usual, but all the input bits to the DAC are 0. In this application, when the reset is canceled, the signal will continue at a phase point where it would be if it had never stopped.

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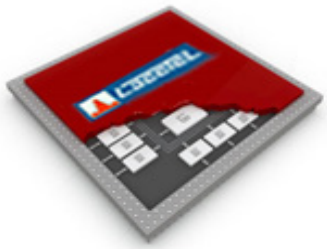

R&D TELECOM INSTITUTE

34515 Independencia Ave., Km 14½, Boyeros, Havana, Republic of Cuba.
www.lacetel.cu